



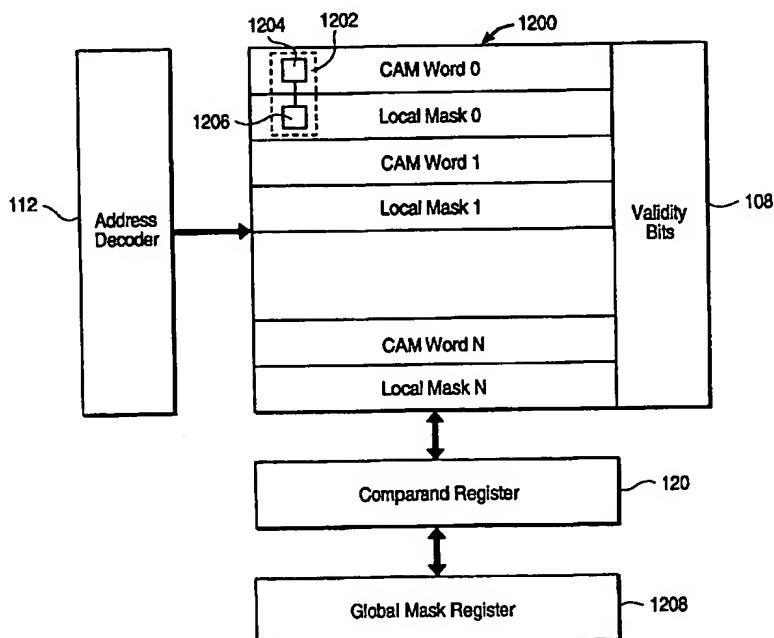
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G11C 15/04		A1	(11) International Publication Number: WO 99/23663
			(43) International Publication Date: 14 May 1999 (14.05.99)
(21) International Application Number: PCT/US98/21853		(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 14 October 1998 (14.10.98)			
(30) Priority Data: 08/967,314 30 October 1997 (30.10.97) US 09/001,110 30 December 1997 (30.12.97) US 09/150,517 9 September 1998 (09.09.98) US			
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(54) Title: SYNCHRONOUS CONTENT ADDRESSABLE MEMORY WITH SINGLE CYCLE OPERATION

(57) Abstract

A content address memory (CAM) device. The CAM device is a synchronous device that may perform all of the following operations all in one clock cycle: (1) receive comparand data from a comparand bus; (2) receive an instruction from an instruction bus instructing the CAM device to compare the comparand data with a first group of CAM cells in a CAM array; (3) perform the comparison of the comparand data with the first group of CAM cells; (4) generate a match address for a location in the CAM array that stores data matching the comparand data; (5) access data stored in a second group of the CAM cells in the CAM array, wherein the second group of CAM cells may store data associated with the matched location; and (6) output to an output bus the match address, the data stored in the second group of CAM cells, and/or status information corresponding to the matched address or the second group of CAM cells. The status information may include a match flag, multiple match flag, full flag, skip bit, empty bit, or a device identification for the CAM device. The CAM array may also include ternary CAM cells that are individually maskable so as to effectively store either a logic one, logic zero, or a don't care state for compare operations.



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SYNCHRONOUS CONTENT ADDRESSABLE MEMORY WITH SINGLE CYCLE OPERATION

This is a continuation-in-part of co-pending U.S. Application No. 08/967,314 filed on October 30, 1997 and entitled "SYNCHRONOUS CONTENT ADDRESSABLE MEMORY WITH SINGLE CYCLE OPERATION".

FIELD OF THE INVENTION

The present invention relates generally to content addressable memory (CAM) devices.

BACKGROUND

A content addressable memory (CAM) device is a storage device that can be instructed to compare a specific pattern of comparand data with data stored in its associative CAM array. The entire CAM array, or segments thereof, are searched in parallel for a match with the comparand data. If a match exists, the CAM device indicates the match by asserting a match flag. Multiple matches may also be indicated by asserting a multiple match flag. The CAM device typically includes a priority encoder to translate the matched location into a match address or CAM index and outputs this address to a status register.

Each CAM cell conventionally includes a comparator and a random access memory (RAM) element. The CAM array may be partitioned into separate segments in which one segment stores CAM or compare data to be compared with the comparand data, and another segment stores associated RAM data corresponding to each of the CAM or compare locations. Once a match between the CAM data and the comparand data is determined, the associated RAM data for the matched location may be output to a status register. The RAM data and/or the CAM data may then be read from the status register.

Conventional CAM devices require more than one clock cycle to perform a write and compare instruction. For example, a typical write and compare instruction requires at least three clock cycles: a first clock cycle to

present a compare instruction and/or comparand data to the CAM device, perform the search, and generate a match flag and multiple match flag signal; a second clock cycle to instruct the CAM device to output the matching CAM address or index; and, a third clock cycle to instruct the CAM device to output the associated data and status information (e.g., skip bit, empty bit, full flag, as well as, match and multiple match flags) for the matched location. With conventional cycle times generally running at 100 nanoseconds (ns), it requires at least 300 ns to complete this process. This generally limits the search rate of conventional CAM devices to approximately 1 to 3 million searches per second. This also generally limits the number of ports, segments, or devices that can be supported by a conventional CAM device in a switch or router environment.

The multi-clock cycle process has generally been required due to the architecture of conventional CAM devices. Most CAM devices include a general purpose bi-directional bus that keeps the pin count of the CAM devices to a minimum (e.g., 44 pins). The bi-directional bus is used to load comparand data and instructions into the CAM device. The bi-directional bus is also used to output the matched address, associated data, and status bits from a status register in the CAM device. Because this bus is shared with so many input and output functions, it requires many clock cycles to multiplex data on the bus.

CAM devices that have separated the general purpose bi-directional bus into a data input bus and a data output bus, still require at least three clock cycles to perform the write and compare operation described above, namely: one clock cycle to load the write and compare instruction and/or load the comparand data and perform the comparison with CAM array; one clock cycle to access the associated data; and, one clock cycle to instruct the CAM device to output the match address, associated data, and/or status information.

As applications for CAM devices increase in speed, there has been a desire for faster CAM devices that have shorter search times, or preferably, can execute a write and compare instruction in a fewer number of clock

cycles. For example, it is desirable to have a CAM device that can be used as an address filter or address translator in an ethernet switch or router that operates at data rates of 100 Megabits per second (Mb/s) to 1 Gigabits per second (Gb/s). It is also desirable to have a CAM device that can be used to implement fast routing tables in Internet Protocol (IP) switches. As the number of ports, segments, or devices that are supported by the switches or routers increases, the time required for the supporting CAM device to perform a write and compare operation (e.g., address filter or translation operation) decreases. For example, to support a 1 Gb/s ethernet switch, a CAM device supporting approximately three ports should advantageously be able to perform a single write and compare instruction in approximately 100 ns or faster. A CAM device supporting approximately six ports should advantageously be able to perform a single write and compare instruction in approximately 50 ns or faster.

SUMMARY OF THE INVENTION

A content address memory (CAM) device is disclosed. The CAM device is a synchronous device that may perform all of the following operations in one clock cycle: (1) receive comparand data from a comparand bus; (2) receive an instruction from an instruction bus instructing the CAM device to compare the comparand data with a first group of CAM cells in a CAM array; (3) perform the comparison of the comparand data with the first group of CAM cells; (4) generate a match address for a location in the CAM array that stores data matching the comparand data; (5) access data stored in a second group of CAM cells in the CAM array, wherein the second group of CAM cells may store data associated with the matched location; and (6) output to an output bus the match address, the data stored in the second group of CAM cells, and/or status information corresponding to the matched address or the second group of CAM cells. The status information may include a match flag, multiple match flag, full flag, skip bit, empty bit, or a device identification for the CAM device. The CAM array may also include ternary CAM cells that are individually maskable so

as to effectively store either a logic one, logic zero, or a don't care state for compare operations.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention are illustrated by way of example and are by no means intended to limit the scope of the present invention to the particular embodiments shown, and in which:

Figure 1 is a block diagram of one embodiment of a CAM device according to the present invention;

Figure 2 is block diagram of one embodiment of the CAM array of Figure 1;

Figure 3 is a block diagram of one embodiment of a CAM cell;

Figure 4 is one embodiment of the CAM cell of Figure 3;

Figure 5 is one embodiment of a method performing a write and compare operation in a single clock cycle;

Figure 6 is a timing diagram for one embodiment of the signals generated by the timing generator of Figure 1;

Figure 7 is one embodiment of the timing generator of Figure 1;

Figure 8 is another embodiment of the timing generator of Figure 1;

Figure 9 is a timing diagram illustrating a pipelined mode of operation for the CAM device of Figure 1;

Figure 10 is one embodiment of the signals output onto the ADS BUS of Figure 1;

Figure 11 is another embodiment of the signals output onto the ADS BUS of Figure 1;

Figure 12 is a block diagram of one embodiment of a ternary CAM array;

Figure 13 is one embodiment of the ternary CAM array of Figure 12;

Figure 14 is a block diagram of one embodiment of a ternary CAM cell;

Figure 15 is a circuit diagram of one embodiment of the ternary CAM cell of Figure 14;

Figure 16 is a circuit diagram of another ternary CAM cell;

Figure 17 is a graph comparing the performance of the ternary CAM cells of Figures 15 and 16;

Figure 18 is a block diagram of another ternary CAM cell;

Figure 19 is a circuit diagram of one embodiment of the ternary CAM cell of Figure 18; and

Figure 20 is another embodiment of a ternary CAM cell.

DETAILED DESCRIPTION

A content addressable memory (CAM) device is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details may not be required to practice the present invention. In other instances, well known circuits and devices are shown in block diagram form to avoid obscuring the present invention unnecessarily. Additionally, the interconnection between circuit elements or blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be single signal lines, and each of the single signal lines may alternatively be buses.

The CAM device of the present invention is a synchronous device that has an instruction bus for receiving instructions, a separate comparand bus for receiving comparand data to be compared with one or more CAM cells of a CAM array, and a separate associated data and status bits bus. The associated data and status bits bus may simultaneously or individually output: a match address or CAM index for a location of the CAM array that matches the comparand data; data stored in one or more of the CAM cells of the CAM array, wherein the data is associated with the matched address; and status information corresponding to the matched address or associated data. The status information may include a match flag, multiple match flag, full flag, skip bit, empty bit, or device identification information for the CAM device.

The CAM device may perform, in a single clock cycle (i.e., a flow through mode), a write and compare instruction that causes the CAM device to: (1) receive comparand data from the comparand bus; (2) receive an instruction from the instruction bus instructing the CAM device to compare the comparand data with a first group of CAM cells in a CAM array; (3) perform the comparison of the comparand data with the first group of CAM cell(s); (4) generate a match address if a location in the CAM array stores data matching the comparand data; (5) access data stored in a second group of CAM cells corresponding to the matched location in the CAM array, wherein the accessed data is associated with the matched address; and (6) output the matched address, the data stored in the second group of CAM cells, and/or the status information to associated data and status bits bus.

The single cycle may have any cycle time. For one embodiment, the single cycle time may be approximately 25 ns and the CAM device may have a search rate of approximately 35 to 45 million searches per second. Thus, the present invention may be very useful in a high-speed (e.g., 100 Mb/s or 1 Gb/s) network bridge or router environment. For example, the CAM device of the present invention may support eight or more ports, segments, or devices in a high-speed ethernet switch or router environment having, for example, a data rate of 1 Gb/s. The CAM device of the present invention may store destination addresses of data packets sent between the segments, ports, or devices in the network.

Figure 1 shows CAM device 100 according to one embodiment of the present invention. CAM device 100 includes three separate ports coupled to three separate buses. The first port is coupled to a comparand bus (CBUS) 138 that may be a bi-directional bus used to provide comparand data to comparand register 120. CBUS 138 may also be used to access device configuration register 136, status register 132, device identification register 121, memory configuration register 106, CAM 102, and one or more mask registers (not shown). CBUS 138 may be any size to accommodate any

number of bits. For one embodiment, CBUS 138 is a 64-bit bus. The first port may have input buffers or registers coupled to CBUS 138.

The second port is coupled to an instruction bus (IBUS) 140 that is used to provide instructions to instruction decoder 128. Instructions may be clocked into instruction decoder 128 from IBUS 140 by one or more clock signals output from clock buffer 124 to bus 144. IBUS 140 may be any size to accommodate any number of bits and any number of instructions. For one embodiment, IBUS 140 is 14 bits wide to accommodate 2^{14} unique possible binary coded instructions. Other encodings may be used. The second port may have input buffers or registers coupled to IBUS 140.

Clock buffer 124 may buffer the external clock signal CLK 178 and provide one or more clock signals to timing generator 126 via bus 180, and may provide one or more clock signals to instruction decoder 128 via bus 144. Clock buffer 124 may also generate clock signals having varying phases and frequencies.

The third port is coupled to an associated data and status bit bus (ADS BUS) 142 that may output matched address data, data from CAM array 104 corresponding to the matched address, and/or status information. ADS BUS 142 may be any size to accommodate any number of bits. For one embodiment, ADS BUS 142 is a 64-bit bus. The third port may have output buffers or registers coupled to ADS BUS 142.

Output multiplexer 134 provides data to ADS BUS 142. Output multiplexer 134 may include output buffers, one or more multiplexers, a selector circuit, registers, or latches. Output multiplexer 134 may receive a matching CAM address or index from priority encoder 116 via bus 146, and may also receive data stored in CAM array 104 via sense amplifiers 122 and bus 152. Additionally, output multiplexer 134 may receive status information including a match flag signal (MF) from priority encoder 116 via line 148, a multiple match flag signal (MMF) from priority encoder 116 via line 150, a full flag signal (FF) from flag logic 130 via line 156, device identification information from device identification register 121 via bus 155, and/or validity bits 108 via bus 157. The status information will be

described in more detail below. Output multiplexer 134 may alternatively or additionally receive the matching CAM address, data stored in CAM array 104 corresponding to the matching CAM address, and/or the status information from status register 132 via bus 158. Configuration register 136 may store one or more programmable bits that may control whether output multiplexer 134 outputs the matching CAM address, CAM array data, and status information from status register 132 (e.g., in a pipelined mode) or from the other circuit elements (e.g., in a single cycle flow through mode). Status register 132 may comprise one or more registers.

CAM device 100 may also include flag logic 130 that may generate a full flag (FF) signal on lines 156 in response to validity bits 108 on bus 157. Flag logic 130 may also generate a match flag signal and a multiple match flag signal on lines 156. The flag(s) may be coupled to output multiplexer 134 and/or status register 132.

CAM device 100 may also include device identification register 121 that may store device identification information that identifies CAM device 100 from other CAM devices in a system. The device identification information may comprise any number of bits or signals. For one embodiment, the device identification information is 16 bits of binary encoded information. Any other encoding format may be used. The device identification information may also be provided to status register 132.

CAM device 100 also includes CAM 102. CAM 102 includes a CAM array 104 that may be organized in any number of rows and columns of CAM cells. CAM 102 may also include validity bits 108 that store information about corresponding locations in CAM array 104. For example, the validity bits for a given row or location in CAM array 104 may include a skip bit and an empty bit. The skip bit may indicate that a particular location in CAM array 104 should be skipped when performing a compare operation with comparand data stored in comparand register 120. The empty bit may indicate that a corresponding location in CAM array 104 is empty. The validity bits also group the CAM cells into four states as indicated in Table 1. A comparison operation may compare comparand

data against any of the locations in CAM array 104 that correspond to a given state.

Table 1

SKIP	EMPTY	STATE
0	0	VALID
0	1	EMPTY
1	0	SKIP
1	1	RAM

Validity bits 108 may be provided (e.g., through sense amplifiers) to output multiplexer 134, status register 132, and/or flag logic 130 via bus 157. Alternatively, validity bits 108 may be generated or decoded in response to a decoded instruction output by instruction decoder 128.

Figure 2 shows one embodiment of CAM array 102 having a plurality of CAM cells 202 organized in any number of rows and columns. For one embodiment, CAM array 102 may include approximately 4k (i.e., 4096) rows and approximately 64 columns of CAM cells 202. For another embodiment, CAM array 102 may include approximately 2k (i.e., 2048) rows and approximately 128 columns of CAM cells 202. The validity bits may also be included in additional rows and columns of CAM cells 202.

Each row of CAM cells 202 is coupled to a match line 204 and a word line 208. Each word line 208 is driven by address decoder 112 to select one or more of CAM cells 202 for writing or reading. Each match line 204 is coupled to match latch 114 that latches the match results of a comparison operation. An individual match line will indicate a match only if all of the CAM cells 202 (actually compared) in that row match the comparand data. The latch results are then provided to priority encoder 116 which generates an address corresponding to at least one of the matched locations. For one embodiment, the matched address is the highest priority match address. The highest priority match address may be the lowest numbered address, the highest numbered address, or any other selected address. Alternatively,

the match address may be the lowest priority match address, or any other predetermined priority.

Each column of CAM cells is coupled to a bit line (BL) 210, a complementary bit line (BLB) 212, a compare line (CL) 214, and a complementary compare line (CLB) 216. BL 210 and BLB 212 are coupled to sense amplifiers 122 that may enable data to be read from or written to CAM cells 202. CL 214 and CLB 216 are coupled to comparand register 120 and provide comparand data to CAM cells 202 for comparison purposes. For alternative embodiments, any other CAM array architecture may be used. For example, CAM array 102 may not include CL 214 and CLB 216; rather, BL 210 and BLB 212 may be coupled to comparand register 120 and may be used to perform a comparison with data stored in CAM cells 202 as generally known in the art. For example, in the first part of a compare cycle, compare data may be provided onto BL 210 and BLB 212 from comparand register 120. In the second part of the compare cycle, BL 210 and BLB 212 may be driven with data to be output from CAM array 104.

Figure 3 shows CAM cell 300 that is one embodiment of a CAM cell 202. CAM cell 300 includes comparator 302 and RAM cell 304. RAM cell 304 is coupled to BL 210, BLB 212, and word line 208, and may be any type of RAM cell. When RAM cell 304 is selected by word line 208, data may be read from or written to RAM cell 304 via bit lines BLB 210 and BLB 212. Comparator 302 is coupled to RAM cell 304, CL 214, CLB 216, and match line 204. Comparator 302 may compare data from comparand register 120 (supplied on CL 214 and CLB 216) with data stored in RAM cell 304 (supplied on lines 218 and 220). Comparator 302 may output the comparison result to match line 204. Comparator 302 may be any type of comparison circuit including an exclusive OR (XOR) or exclusive NOR (XNOR) gate. The comparison and read functions of CAM cell 300 may be performed simultaneously or sequentially. In alternative embodiments (e.g., CL 214 and CLB 216 omitted), the comparison and read functions may be performed sequentially. It will be appreciated that numerous other CAM cells may be used for CAM cells 202.

Figure 4 shows CAM cell 400 that is one embodiment of CAM cell 300 of Figure 3 and/or one embodiment of a CAM cell 202 of Figure 2. It will be appreciated that other CAM cells may be used form CAM cell 300 and/or CAM cell 202. CAM cell 400 includes a RAM cell 404 and a comparator 402. RAM cell 404 includes cross-coupled inverters 406 and 408 coupled to nodes 428 and 430. Inverters 406 and 408 may be any type of inverters including NMOS, PMOS, or CMOS inverters with active or passive loads. Ram cell 404 also includes pass gates 410 and 412. Pass gate 410 may be an NMOS transistor having its source (drain) coupled to node 428, its drain (source) coupled to BL 210, and its gate coupled to word line 208. Pass gate 412 may be an NMOS transistor having its source (drain) coupled to node 430, its drain (source) coupled to BLB 212, and its gate coupled to word line 208. When word line 208 is selected (e.g., pulled to a high logic state), pass gate 410 is enabled to transfer data between node 428 and BL 210, and pass gate 412 is enabled to transfer data between node 430 and BLB 212.

Comparator 402 includes transistors 414, 416, 418, and 420. Transistor 414 has its gate coupled to node 428, its source coupled to line 426, and its drain coupled to the source of transistor 416. Transistor 416 has its drain coupled to match line 204, and its gate coupled to CLB 216. Transistor 420 has its gate coupled to node 430, its source coupled to line 426, and its drain coupled to the source of transistor 418. Transistor 418 has its drain coupled to match line 204, and its gate coupled to CL 214. Line 426 may be driven to a voltage VREFL of approximately one threshold voltage above ground (e.g., from approximately 0.6 volts to approximately 0.8 volts) due to the diode configuration of NMOS transistor 422 having its source coupled to ground, and its drain and gate coupled to line 426. One transistor 422 may be used for more than one CAM cell in CAM array 104. Alternatively, VREFL may be driven to approximately zero volts to approximately one volt by a reference voltage generator or other circuitry. For an alternative embodiment, line 426 may be directly connected to ground.

CAM cell 400 may also include PMOS transistor 424 that may pull match line 204 towards VDD when there is no match between data stored in

RAM cell 404 and comparand data provided on compare lines CL 214 and CLB 216. PMOS transistor 424 has its source coupled to VDD, its drain coupled to match line 204, and its gate coupled to a reference voltage VREFH. VREFH may be approximately one threshold drop below VDD (e.g., approximately 0.6 to 0.8 volts below VDD). Alternatively, VREFH may be other voltage. VDD may be any supply voltage. For example, VDD may be from approximately 2.7 volts to approximately 7.0 volts.

The operation of CAM cell 402 may be illustrated as follows. Assume that RAM cell 404 stores a high logic state (a one) at node 428 causing transistor 414 to be on. The cross-coupled nature of inverters 406 and 408 will cause a low logic state (a zero) to be stored at node 430 turning off transistor 420. During a compare operation, if the comparand data is also high (CL 214 high), then CLB 216 will be driven low causing transistor 416 to turn off. Therefore, if there is a match between the comparand data and the data stored by RAM cell 404, match line 204 will remain in a high state. If, however, the comparand data is low (CL 214 low), then CLB 216 is driven high causing transistor 416 to be on and match line 204 to be pulled towards the potential of line 426 via transistors 414 and 416. Therefore, if there is no match between the comparand data and the data stored by RAM cell 404, match line 204 will be pulled to a low state.

Similarly, if RAM cell 404 stores a low logic state at node 428, transistor 414 will be off, and transistor 420 will be on. During a compare operation, if the comparand data is also low, then CL 214 will be driven low causing transistor 418 to turn off. Therefore, if there is a match between the comparand data and the data stored by RAM cell 404, match line 204 will remain in a high state. If, however, the comparand data is high, then CL 214 is driven high causing transistor 418 to be on and match line 204 to be pulled towards the potential of line 426 via transistors 418 and 420. Therefore, if there is no match between the comparand data and the data stored by RAM cell 404, match line 204 will be pulled to a low state.

Because of the separate bit lines and compare lines, CAM cell 400 may perform a comparison operation at the same time that data is read from

RAM cell 404. That is, data may be compared on lines CL 214 and CL 216 with nodes 428 and 430 at the same time that data is read from nodes 428 and 430 to BL 210 and BL 212, respectively. This may be advantageous in performing compare operations in CAM devices such as CAM device 100 of Figure 1.

With respect to Figure 2, CAM array 104 may store associative memory data or compare data (e.g., port address, pattern recognition keys, etc.) in any number of CAM cells 202 in a given row of CAM cells. The compare data may be compared with comparand data stored in comparand register 120. Similarly, CAM array 104 may store associated data or RAM data (e.g., bridge or switch port address, access information, or aging data) in any number of CAM cells 202 in a given row of CAM cells. The associated data may correspond to, or be associated with, other CAM cells in the same row that store compare data. The CAM cells 202 may be partitioned with a granularity of one into compare data and associated data segments. The compare data and associated data segments may be interleaved, or they may be non-interleaved segments.

For one embodiment, memory configuration register 106 may be used to program which bits in CAM array 104 are used to store compare data, and which bits are used to store associated data or other information. Memory configuration register 106 may thus act as a mask register indicating which CAM cells 202 (e.g., that may store compare data) will participate in a compare operation with comparand data, and which bits (e.g., that may store associated data or any other information) will not participate in a comparison operation with comparand data. For example, memory configuration register 106 may include one or more programmable bits corresponding to each column of CAM cells in CAM array 104. Each bit may be programmed via CBUS 138.

Data stored in CAM array 104 may be output (e.g., via sense amplifiers 122 and output multiplexer 134) in any order or in any format. For one embodiment, CAM array 104 may output its contents in multi-bit segments. Each segment may store compare data, associated data, and/or

other information. For one example, CAM array 104 may be partitioned into four segments of 16 bits each. One or more of the segments may be sensed and output by output multiplexer 134 in any order (e.g., 2^4 or 16 possible ordered outputs). One or more bits in device configuration register 136 may be programmed via CBUS 138 to cause one or more multiplexers in output multiplexer 134 to output the desired order of the segments to ADS BUS 142. For example, programming a bit in device configuration register 136 may cause a first 16-bit segment to be output on the first sixteen lines of ADS BUS 142, and a second 16-bit segment to be output on the second sixteen lines of ADS BUS 142. For this example, the remaining signal lines of ADS BUS 142 may output a match address and status information as shown in Figure 10. For another example, programming a bit in device configuration register 136 may cause a third 16-bit segment to be output on the first sixteen lines of ADS BUS 142, and a fourth 16-bit segment to be output on the second sixteen lines of ADS BUS 142.

Figure 5 describes one embodiment 500 of generally performing a write and compare instruction in CAM device 100 in one clock cycle of external clock signal CLK 178. At the start of the clock cycle, instruction decoder 128 decodes the write and compare instruction on IBUS 140 at step 502. In response to the instruction, comparand register 120 loads comparand data from CBUS 138 at step 504. Instruction decoder 128 may include a look-up table, a state machine, or any other control logic that can decode the write and compare or a compare instruction on IBUS 140.

At step 506, the comparand data in comparand register 120 is compared with data stored in CAM array 104 to determine if there is a match. The write and compare instruction decoded by instruction decoder 128 may instruct CAM device 100 to compare the comparand data against all entries, only valid entries (e.g., skip and empty bits inactive), entries where the skip bits are active, or entries where the skip bit and empty bits are active. The write and compare instruction may also instruct CAM device 100 to use one or more mask registers (not shown) to mask certain columns of CAM cells from the comparison. Alternatively, the decoded write and

compare instruction may instruct CAM device 100 to compare the comparand data against associated data stored in CAM array 104. The write and compare instruction may be binary encoded on IBUS 140, or may be encoded in any other format. The comparison results of step 506 will be reflected by the state of the match lines 204 in CAM array 104.

At step 508, the states of the match lines in CAM array 104 are latched by match latch 114 and provided to priority encoder 116. At step 510, priority encoder 116 determines the highest priority match address from the comparison. Match latch 114 may be incorporated into priority encoder 116. The match address is then output by priority encoder 116 to bus 146 and may be latched by address latch 118. Bus 146 couples the match address to output multiplexer 134 and status register 132 for output to ADS BUS 142. As generally known in the art, priority encoder 116 may also generate a match flag signal on line 148 if there is at least one match between the comparand data and the data stored in CAM array 104. Additionally, priority encoder 116 may also generate a multiple match flag signal on line 150 if there is at least two matches between the comparand data and the data stored in CAM array 104.

The match address on bus 162 is provided to address decoder 112 by address selector 110. Address selector 110 couples either the address on address bus 164 or the match address on bus 162 to address decoder 112 in response to a signal on line 166. Address bus 164 may be an internal bus within CAM device 100 (e.g., coupled to an address counter) or a bus external to CAM device 100. Address selector 110 may be a multiplexer. For an alternative embodiment, address selector 110 may be omitted and bus 162 may be directly connected to address decoder 112.

At step 512, address decoder 112 decodes the match address and selects one row of CAM cells in CAM array 104 corresponding to the match address. Address decoder 112 may also select the corresponding validity bits 108 for the selected row in CAM array 104. At step 514, one or more CAM cells at the high priority match address are sensed by sense amplifiers 122 and coupled to bus 152 for output to ADS BUS 142 via output multiplexer

134. Additionally, the validity bits may be accessed and/or sensed (e.g., by sense amplifiers 122) and output to bus 157. At step 516, and before the end of the first clock cycle of external clock CLK 178, output multiplexer 134 may simultaneously or concurrently output to ADS BUS 142: the data read from CAM array 104 onto bus 152; the match address on bus 146; and/or, the status information (e.g., match flag signal on line 148, multiple match signal on line 150, full flag signal on line 156, the validity bits on bus 157, and/or device identification information from device identification register 121 on bus 155). For example, output multiplexer 134 may output the signals as illustrated in Figures 10 and 11.

Timing generator 126 outputs timing signals on lines 160, 166, 168, 170, 172, 174, 176, and 182 in response to one or more clock signals from clock buffer 124 and an indication of the write and compare instruction (or simply a compare instruction) from instruction decoder 128 on bus 159. The timing signals coordinate the operation of the various circuit elements to perform the write and compare instruction in one clock cycle.

Figure 6 is an illustrative timing diagram showing one embodiment of the sequence of signals generated by timing generator 126 for a write and compare instruction. At time t_0 , the start of the clock cycle of CLK 178, instruction decoder 128 decodes the write and compare instruction on IBUS 140 and sends a signal on bus 159 to timing generator 126. In response, timing generator 126 sends a pulse signal on line 160 to cause the comparand data on CBUS 138 to be loaded into comparand register 120.

Between times t_0 and t_1 , the comparand data is provided to CAM array 104 and compared against one or more CAM cells of CAM array 104 for a match. The match results reflected on the match lines of CAM array 104 are then coupled to match latch 114 and latched by the pulse generated at time t_1 on line 172. The latched match signals are coupled to priority encoder 116.

At time t_2 , timing generator 126 generates a pulse on line 174 that causes priority encoder 116 to generate a match address for the highest priority matched location. The highest priority match address is output to

bus 146. At time t3, timing generator 126 generates a pulse signal on line 176 that causes address latch 118 to latch the match address from priority encoder 116 and provide the latched match address to bus 162. For an alternative embodiment, the match address may be provided to address selector 110 without being latched by address latch 118.

At time t4, timing generator 126 generates a pulse signal on line 166 that causes optional address selector 110 to couple the match address on bus 162 to address decoder 112. Address decoder 112 may then decode the match address and select the row of CAM cells in CAM array 104 and/or the validity bits 108 that corresponds to the matched address. Address decoder 112 may alternatively be synchronous and start decoding the match address in response to the signal on line 166. Alternatively, address decoder 112 may start decoding the match address in response to a pulse signal on line 168. The pulse signal on line 168 may be generated coincident with the pulse signal on line 166, or after the pulse signal on line 166 but before the pulse signal on line 170.

Between times t4 and t5, sense amplifiers 122 sense the selected CAM cells of CAM array 104 (and/or the corresponding validity bits). At time t5, timing generator 126 then generates a pulse signal on line 170 that causes sense amplifiers 122 to latch the sensed data and couple this data to bus 152. This data may then be output by output multiplexer 134 to ADS BUS 142 by time t6 along with the match address from bus 146 and the status information (e.g., the validity bits 108, the match flag signal from line 148, the multiple match flag signal from line 150, the full flag signal on line 156, and/or the device identification on bus 155). A subsequent instruction (e.g., another write and compare instruction) may then begin at time t6.

Timing generator 126 may additionally generate one or more pulse signals on bus 182 at time t6 that causes status register 132 to load the match address from bus 146, the match flag signal from bus 148, the multiple match flag signal from line 150, the device identification information from bus 155, the sensed data CAM array data on bus 152, the full flag signal from

line 156, and/or validity bits 108 from bus 157. The signals on bus 182 may alternatively be generated by instruction decoder 128.

The time differences between the pulses generated on lines 160, 172, 174, 176, 166, 170, and 182 are sufficient to allow the operations described above to function properly under anticipated, characterized, or specified process, temperature, and supply voltage ranges. For one embodiment, the clock cycle time (i.e., t_6-t_0) is approximately 25 ns, t_1-t_0 is approximately 4 ns, t_2-t_1 is approximately 2 ns, t_3-t_2 is approximately 5 ns, t_4-t_3 is approximately 2 ns, t_5-t_4 is approximately 4 ns, and t_6-t_5 is approximately 3 ns. For other embodiments, the time differences between the pulse signals may be different values.

The signals generated on lines 160, 172, 174, 176, 166, 170, and 182 are shown in Figure 6 as pulse signals. For alternative embodiments, a rising or falling edge of a signal may be generated instead of a pulse signal. The pulse signals may also be programmable or adjustable to have any pulse width.

Timing generator 126 may be any timing generator circuit that generates the pulses on lines 160, 172, 174, 176, 166, 170, and 182 at the appropriate times. Figure 7 shows timing generator 700 that is one embodiment of timing generator 126 of Figure 1. Timing generator 700 includes control logic 702 that receives one or more clock signals on bus 180 from clock buffer 124, and an indication of the write and compare instruction from instruction decoder 128 on bus 159. Control logic 702 may be a pulse generator circuit that generates a pulse signal on line 710 that may be coupled to line 160. The pulse signal on line 710 may be delayed by a series of delay elements 704, 705, 706, 707, 708, and 709 that may be used to generate the pulse signals on lines 172, 174, 176, 166, 170, and 182, respectively. Delay elements 704-709 may include, for example, resistors, capacitors, transistor pass gates, inverting buffers, and/or non-inverting buffers. Each delay element may also include a programmable element that enables a user or manufacturer to program the delay of each of the delay elements so that the pulses on lines 172, 174, 176, 166, 170, and 182 may be

generated at the appropriate times. The programmable elements may also program the pulse width of one or more of the signals 172, 174, 176, 166, 170, and 182.

For an alternative embodiment, clock buffer 124 may generate a plurality of signals at different times, and timing generator 126 may include circuitry that selectively enables each of the clock signals to be coupled to lines 160, 172, 174, 176, 166, 170, and 182 at the appropriate time.

For still another embodiment, clock buffer 124 may generate a clock signal on bus 180 that has a frequency that is n times the frequency of CLK 178, where n is greater than one. Timing generator 126 may be a state machine or counter that consecutively generates the signals on lines 160, 172, 174, 176, 166, 170, and 182 once per clock cycle of the clock signal on bus 180.

Figure 8 illustrates timing generator 800 that is another embodiment of timing generator 126 of Figure 1. Timing generator 800 includes a clock generator 802 and latches 803-808. Clock buffer 802 generates one or more clock signals on bus 816 in response to one or more buffered clock signals received on bus 180 from clock buffer 124. Alternatively, clock generator 802 may receive CLK 178. The clock signals on bus 816 may be pulse signals or edge transitions, and may be of any pulse width. For one embodiment, the clock signals on bus 816 include pulse signals that are approximately 2 to 6 ns in duration. The clock signals from bus 816 are provided to the clock inputs of latches 803-808. For example, one or more clock signals on lines 810, 811, 812, 813, 814, and 815 are coupled to the clock inputs of latches 803, 804, 805, 806, 807, and 808, respectively. The signals on lines 810-815 may be the same signal or different signals. For one embodiment, the signals on lines 810-815 may be pulse signals that start at the beginning of a clock cycle, the middle of clock cycle, at the end of a clock cycle, or at any other predetermined time within a clock cycle. Latches 803, 804, 805, 806, 807, and 808 may be self-timed latches that generate pulse signals on lines 172, 174, 176, 166, 170, and 182, respectively, in response to data input signals on lines

820-825 and the assertion of clock signals on lines 810-815. Lines 820-825 may be included in bus 159 output by instruction decoder 129 of Figure 1.

With respect to Figures 6 and 8, clock generator 802 may generate the signal on line 160 at time t_0 . The signal on line 160 may alternatively be generated by a latch device, but it may be advantageous to generate this signal very close to the rising edge transition of CLK 178. For one embodiment, CLK 178 may be provided on line 160. After the write and compare instruction is decoded, instruction decoder 128 may assert signals on lines 820-825 that cause the pulses on lines 172, 174, 176, 166, 170, and 182 to be generated. Latch 803 may latch the signal on line 820 in response to a clock signal on line 810. The signal on line 810 may arrive at time t_1 , or latch 803 may receive the signal on line 810 earlier and may delay the generation of the signal on line 172 until time t_1 . Latch 804 may latch the signal on line 821 in response to a clock signal on line 811. The signal on line 811 may arrive at time t_2 , or latch 804 may receive the signal on line 811 earlier and may delay the generation of the signal on line 174 until time t_2 . Latch 805 may latch the signal on line 822 in response to a clock signal on line 812. The signal on line 812 may arrive at time t_3 , or latch 805 may receive the signal on line 812 earlier and may delay the generation of the signal on line 176 until time t_3 . Latch 806 may latch the signal on line 823 in response to a clock signal on line 813. The signal on line 813 may arrive at time t_4 , or latch 806 may receive the signal on line 813 earlier and may delay the generation of the signal on line 166 until time t_4 . Latch 807 may latch the signal on line 824 in response to a clock signal on line 814. The signal on line 814 may arrive at time t_5 , or latch 807 may receive the signal on line 814 earlier and may delay the generation of the signal on line 170 until time t_5 . Latch 808 may latch the signal on line 825 in response to a clock signal on line 815. The signal on line 815 may arrive at time t_6 , or latch 808 may receive the signal on line 815 earlier and may delay the generation of the signal on line 182 until time t_6 . There may be one more latches 808 to output one or more signals on one or more lines 182.

The previous embodiments have described a single clock cycle operation of a write and compare instruction. The CAM device 100 of Figure 1 may also perform a compare instruction in a single cycle. The compare instruction performs the same steps as the write and compare operation described above excluding the additional step of loading the comparand data into comparand register 120.

CAM device 100 may also function in a pipelined mode of operation to take advantage of the fact that CAM device 100 can perform a write and compare instruction (or simply a compare instruction) in a single clock cycle. An example of a pipelined mode of operation is illustrated in Figure 9. At time t_0 , a first write and compare instruction is provided to CAM device 100 on bus 140 at the same time that first comparand data is provided on CBUS 138 for comparand register 120. During clock cycle t_{cycle1} , all of the steps of the process of Figure 5 and/or Figure 6 are performed by CAM device 100. By the end of t_{cycle1} , status register 132 receives the match address on bus 146, the match flag signal on line 148, the multiple match flag signal on line 150, the full flag signal on line 156, the device identification information on bus 155, the data read from CAM array 104 on bus 152, and/or validity bits 108 on bus 157. Status register 132 may be updated with this information by one or more signals on bus 182 from timing generator 126 or clock buffer 124.

The rising edge of CLK 178 at time t_1 may clock the contents of status register 132 onto ADS BUS 142 via output multiplexer 134 at time t_2 . Output multiplexer 134 may be configured to output the data from status register 132 rather than bypass the status register 132 by programming one or more bits in configuration register 136. Figure 10 shows one embodiment of the data output on ADS BUS 142 from status register 132 via output multiplexer 134 when ADS BUS is a 64-bit bus. Figure 11 shows another embodiment. For alternative embodiments, the data output from status register 132 may be in any other format or order. For yet other embodiments, there may be more than one status register 132 to further pipeline the data to be output to ADS BUS 142.

The time difference between times t_1 and t_2 may be very fast because it is the time to clock a register element. For one embodiment, the time difference between t_1 and t_2 may be approximately 2 - 10 ns. Additionally, the data output to ADS BUS 142 from status register 132 may be valid for a large percentage of the clock cycle time (e.g., approximately 30 percent to approximately 90 percent) as the data will become invalid only at the end of the next clock cycle t_{cycle2} .

At the end of clock cycle t_{cycle1} and the start of clock cycle t_{cycle2} , a second write and compare instruction (or simply a compare instruction) may be provided on IBUS 140 along with second comparand data on CBUS 138. During clock cycle t_{cycle2} , all of the steps of the process of Figure 5 and/or Figure 6 are performed by CAM device 100. By the end of t_{cycle2} , status register 132 receives the match address on bus 146, the match flag signal on line 148, the multiple match flag signal on line 150, the full flag signal on line 156, the device identification information on bus 155, the data read from CAM array 104 via bus 152, and/or validity bits 108 on bus 152. This information will then be available from status register 132 in clock cycle t_{cycle3} .

CAM array 104 of CAM device 100 may also operate as a ternary CAM array and perform the "write and compare" or compare operations described above in a single clock cycle or less than three clock cycles. A ternary CAM device is a CAM device that can effectively store three states of information, namely: a logic one state, a logic zero state, and a don't care state for compare operations. This provides more flexibility in the use of CAM device 100.

Figure 12 shows ternary CAM array 1200 that is one embodiment of CAM array 104 of Figure 1. Each CAM word in ternary CAM array 1200 has an associated local mask word that stores masking data for the CAM word. For example, local mask word zero stores masking data for the CAM cells in CAM word zero, and local mask word N stores masking data for the CAM cells in CAM word N.

In contrast to global mask registers (e.g., global mask register 1208) that mask entire columns of CAM cells, the local mask word is used to mask individual CAM cells of a corresponding CAM word on a bit-by-bit basis. Thus, each CAM cell/local mask cell pair (e.g., CAM cell 1204 and local mask cell 1206) may be considered to be a mask-per-bit CAM cell such as mask-per-bit CAM cell 1202 of Figure 12.

Local mask information can be written to each of the local mask words directly from comparand bus 138, from comparand register 120, a global mask register (not shown), or from other storage locations in CAM device 100. The local mask locations may be selected for writing by address decoder 112 and the local mask locations may be sequentially or randomly selected to receive local mask data. The local mask data may also be read via sense amplifiers 170 and may be provided to status register 132, output multiplexer 134, ADS BUS 142, comparand register 120, a global mask register, or any other storage element in CAM device 100.

For one embodiment, the local mask cells are volatile mask cells that need to be updated after power up of CAM device 100. The local mask cells may also be updated when the corresponding CAM cells are updated, or at any other time. For another embodiment, the local mask cells may be other types of memory cells including nonvolatile memory cells. Alternatively and/or additionally, the local mask cells may be resettable to a predetermined state, for example, after power-up or by other means.

Figure 13 shows ternary CAM array 1300 that is one embodiment of ternary CAM array 1200 of Figure 12. Ternary CAM array 1300 includes CAM words that each include a row of any number of CAM cells 1302, and local mask words that each include a row of any number of mask cells 1304. The validity bits may also be included in additional rows and columns of CAM cells 1302. Each CAM cell 1302 is coupled to match line 1314, word line 1316, bit line BL 1306, and the logical complement of bit line BLB 1308. Each local mask cell 1304 is coupled to a corresponding CAM cell 1302, BL 1306, BLB 1308, comparand line CL 1312, the logical complement of the comparand line CLB 1310, and a mask word line 1318. The comparand lines

provide comparand data to the CAM cells 1302 for comparison with the data stored in the CAM data. Although CL 1312 and CLB 1310 are shown as providing data to local mask cells 1304, in alternative embodiments, CAM cells 1302 may additionally or alternatively receive comparand data from CL 1312 and CLB 1310. Additionally, while ternary CAM 1300 shows columns of CAM cells 1302 and mask cells 1304 coupled to common bit lines, in an alternative embodiment, mask cells 1304 may be coupled to separate mask bit lines. Additionally and/or alternatively, word lines 1316 and 1318 may be the same word line.

Each word line 1316 is driven by address decoder 112 to select one or more of CAM cells 1302 for writing or reading. Similarly, each mask word line 1318 is driven by address decoder 112 to select one or more of local mask cells 1304 for writing or reading. Address decoder 112 may drive either the word lines 1316 or the mask word lines 1318 in response to the appropriate instruction decoded by instruction decoder 128 of Figure 1.

Each CAM cell 1302/local mask cell 1304 pair may be considered a mask-per-bit CAM cell in which the local mask cell 1304 is used to store mask data for its corresponding CAM cell. An exemplary mask-per-bit CAM cell 1320 is shown as including CAM cell 1302 and local mask cell 1304. For alternative embodiments, local mask cell 1304 may be used to store masking data corresponding to more than one CAM cell 1302.

Figure 14 shows mask-per-bit ternary CAM cell 1400 that is one embodiment of mask-per-bit ternary CAM cell 1320 of Figure 13. CAM cell 1400 includes CAM cell 1402 and local mask cell 1404. CAM cell 1402 includes memory cell 1406 and compare circuit 1408. Memory cell 1406 stores data to be compared with comparand data provided on CL 1310 and CLB 1312 during a compare operation. Memory cell 1406 may be any volatile or nonvolatile memory cell. When memory cell 1406 is selected by word line 1316, data may be read from or written to memory cell 1406 via BL 1306 and BLB 1308. Compare circuit 1408 is coupled to memory cell 1406 and compares the data stored in memory cell 1406 with data provided by masking circuit 1410 on lines 1416 and 1417. Compare circuit 1408 outputs

the comparison result to match line 1314. Compare circuit 1408 may be any type of comparison circuit including an exclusive OR (XOR) or exclusive NOR (XNOR) gate.

Local mask cell 1404 includes masking cell 1412 and masking circuit 1410. Masking cell 1412 stores masking data that indicates whether the data stored in memory cell 1406 will be masked during a comparison operation. For one embodiment, masking cell 1412 may be any volatile or nonvolatile memory cell. When masking cell 1412 is selected by mask word line 1318, masking data may be read from or written to masking cell 1412 via BL 1306 and BLB 1308. Masking circuit 1410 receives the masking data from masking cell 1412 over lines 1418 and 1419 and in response thereto determines whether the comparand data on CL 1310 and CLB 1312 or masked data is provided to compare circuit 1408 on lines 1416 and 1417. For example, when the masking data stored in masking cell 1412 indicates that the data in memory cell 1406 should be masked from a comparison with the comparand data provided on CL 1310 and CLB 1312, masking circuit 1410 provides masked data to compare circuit 1408 such that compare circuit 1408 indicates a match to match line 1314 regardless of whether the data stored in memory cell 1406 matches the comparand data. The masked data provided on lines 1416 and 1417 may be any predetermined data. For one embodiment, the masked data may be the same or the logical complement of the masking data provided by masking cell 1412 on lines 1418 and 1419.

When the masking data stored in masking cell 1412 indicates that the data stored in memory cell 1406 should not be masked from a comparison with the comparand data, masking circuit 1410 provides the comparand data to compare circuit 1408 to compare with the data stored in memory cell 1406.

Thus, in response to the masking data stored in masking cell 1412, masking circuit 1410 either provides the comparand data or masked data to compare circuit 1408. Conventional mask-per-bit ternary CAM cells generally include a masking element between compare circuitry and the match line and thus mask the comparison result. This tends to slow down

the operation of the CAM cell. In contrast, ternary CAM cell 1400 determines the data that is actually compared and may increase the operating speed of CAM cell 1400 in determining the state of match line 1314.

While two signal lines are shown for interfacing between memory cell 1406 and compare circuit 1408 (i.e., lines 1414 and 1415), compare circuit 1408 and masking circuit 1410 (i.e., lines 1416 and 1417), and masking circuit 1410 and masking cell 1412 (i.e., lines 1418 and 1419), any number of signal lines may be used.

Figure 15 shows mask-per-bit ternary CAM cell 1500 that is one embodiment of CAM cell 1400 of Figure 14. CAM cell 1500 includes memory cell 1506, compare circuit 1508, masking circuit 1510, and masking cell 1512 which are exemplary embodiments of circuits 1406, 1408, 1410, and 1412, respectively. Other embodiments may be used.

Memory circuit 1506 includes two cross-coupled inverters 1526 and 1528 that form a bi-stable latch to store data nodes 1521 and 1523. Data may be communicated between the bi-stable latch and BL 1306 and BLB 1308 via pass gates 1522 and 1524, respectively. Pass gates 1522 and 1524 are controlled by word line 1316. For alternative embodiments, any other type of volatile or nonvolatile memory cell may be used. The data stored by memory cell 1506 is passed on lines 1514 and 1515 to compare circuit 1508 for comparison with the data output by masking circuit 1510.

Masking cell 1512 includes two cross-coupled inverters 1546 and 1548 that form a bi-stable latch to store masking data nodes 1545 and 1547. The masking data is communicated between BL 1306 and BLB 1308 via pass gates 1546 and 1548 that are controlled by mask word line 1318. The masking data stored by the bi-stable latch indicates whether masked data or comparand data is provided to compare circuit 1508 for comparison.

The masking data is provided to masking circuit 1510 on lines 1518 and 1519. Masking circuit 1510 includes transistors 1538 and 1540 that determine whether masked data or comparand data is provided to line 1516 in response to the masking data on lines 1518 and 1519. Transistor 1538 has

its source (drain) coupled to CLB 1312, its drain (source) coupled to line 1516, and its gate coupled to line 1519. Transistor 1540 has its drain coupled to line 1516, its source coupled to ground, and its gate coupled to line 1518. Masking circuit 1510 further includes transistors 1542 and 1544 that determine whether masked data or comparand data is provided to line 1517 in response to the masking data on lines 1518 and 1519. Transistor 1544 has its source (drain) coupled to CL 1310, its drain (source) coupled to line 1517, and its gate coupled to line 1519. Transistor 1542 has its drain coupled to line 1517, its source coupled to ground, and its gate coupled to line 1518.

Compare circuit 1508 includes two sets of transistors to compare the data output by memory cell 1506 on signal lines 1514 and 1515 with the data output by masking circuit 1510 on lines 1516 and 1517. The first set of transistors includes transistors 1530 and 1532. Transistor 1530 has its source coupled to ground, its drain coupled to the drain (source) of transistor 1532, and its gate coupled to signal line 1514. Transistor 1532 has its source (drain) coupled to match line 1314 and its gate coupled to signal line 1516. The second set of transistors includes transistors 1534 and 1536. Transistor 1534 has its source coupled to ground, its drain coupled to the drain (source) of transistor 1536, and its gate coupled to signal line 1515. Transistor 1536 has its gate coupled to signal line 1517 and its source (drain) coupled to match line 1314. Match line 1314 may be precharged to a voltage approximately equal to a power supply voltage VDD by precharge circuit 1520.

The operation of CAM cell 1500 may be illustrated as follows. When masking is disabled, masking cell 1512 provides a logic zero signal on line 1518 to turn off transistors 1540 and 1542, and further provides a logic one signal on line 1519 to enable transistors 1538 and 1544 to provide comparand data from CLB 1312 and CL 1310 to lines 1516 and 1517, respectively. Thus, when masking is disabled, compare circuit 1508 may compare the data on lines 1514 and 1515 with the comparand data from CLB 1312 and CL 1310, respectively. If there is a match, neither set of transistors in compare circuit 1508 will provide a path to ground and the state of match line 1314 will remain unaltered. If there is no match, match line 1314 will be discharged

towards ground through at least one of the sets of transistors in compare circuit 1508.

When masking is enabled, masking cell 1512 provides a logic zero signal on line 1519 to turn off transistors 1538 and 1544 such that the comparand data is not provided to signal lines 1516 and 1517. Additionally, masking cell 1512 provides a logic one signal on signal line 1518 to turn on transistors 1540 and 1542 and pull lines 1516 and 1517 towards a ground potential. When signal lines 1516 and 1517 are pulled towards a ground potential, transistors 1532 and 1536 are turned off such that no path to ground is available in compare circuit 1508 regardless of whether the comparand data on CLB 1312 and CL 1310 matches the data stored by memory cell 1506. Thus, CAM cell 1500 effectively stores a don't care state for the compare operation.

CAM cell 1500 may provide a speed advantage in resolving the state of match line 1314 over other ternary CAM architectures. One example of another ternary CAM 1600 is shown in Figure 16 which includes a memory circuit 1606, compare circuit 1608, mask cell 1612, and masking transistor 1610. Compare circuit 1608 compares the data stored in memory cell 1606 with the comparand data on CLB and CL and provides the compare result to node 1622. Mask cell 1612 stores masking data that controls masking transistor 1610. Masking transistor 1610 determines whether the comparison result at node 1622 is provided to match line 1620. Consider the case where masking is disabled (transistor 1610 on), and data provided on line 1615 is a logic zero. During a compare operation, if CLB provides a logic one to transistor 1632 (a matching condition) nodes 1622 and 1633 will each charge to VDD minus a threshold voltage (V_T) of NMOS transistors 1610 and 1632, respectively. During a subsequent mismatching cycle, nodes 1633 and 1622 will need to be discharged along with match line 1614. Thus, ternary CAM cells that place the masking circuit in between the compare circuit and the match line to gate the match result can result in undesirable charged nodes that must be discharged when a mismatch is determined.

In contrast to CAM cell 1600, CAM cell 1500 uses masking circuit 1510 to determine the data supplied to compare circuit 1508. Masking circuit 1510 is not used to gate a completed comparison to match line 1314. Thus, match line 1314 may be charged and discharged faster than other ternary CAM cell architectures. For example, consider the case where match line 1314 is initially precharged to a high logic state and one or more ternary CAM cells such as CAM cell 1500 indicate a non-masked matching condition. During a comparison operation, the non-masked matching cells will each have an intermediate node 1533 or 1535 that will charge to approximately $V_{DD}-2V_T$, while node 1537 remains precharged to approximately V_{DD} by precharge circuit 1520. If one of the ternary CAM cells coupled to the same match line subsequently indicates a non-masked mismatching condition in a subsequent compare operation, then the non-masked mismatching cell will need to discharge match line 1314 and the intermediate nodes 1533 (and/or 1535) of the non-masked matching cells. Note that only one intermediate node 1533 or 1535 will have to be discharged rather than two intermediate nodes as illustrated in ternary CAM cell 1600 of Figure 16. Similarly, if the non-masked mismatching cell subsequently indicates a non-masked matching condition in a subsequent compare operation, then only one intermediate node 1533 or 1535 will need to be charged to $V_{DD}-2V_T$ by the precharge circuit 1620. This can result in a significant decrease in the time required to resolve the state of match line 1314 and thus may result in a significant decrease in the time required to generate a match flag for the CAM device.

The graph in Figure 17 shows exemplary simulation data taken for one embodiment of CAM cells 1500 and 1600 at a V_{DD} of approximately 3.14 volts. As the graph illustrates, the speed increase (Δt_1) in discharging a match line for a non-masked non-matching condition is approximately 2.3 nanoseconds (ns) at 1.5 volts for CAM cell 1500 over CAM cell 1600. The graph further illustrates that the speed increase (Δt_2) in charging a match lines for a non-masked matching condition is approximately 3.8 nanoseconds (ns) at 1.5 volts for CAM cell 1500 over CAM cell 1600.

The response time of CAM cell 1500 may be further increased by placing PMOS transistors across transistors 1538 and 1544. For example, a PMOS transistor may have source (drain) coupled to the source (drain) of transistor 1538 and CLB 1312, its drain (source) coupled to the drain (source) of transistor 1538 and signal line 1516, and its gate coupled to signal line 1518. A similarly configured PMOS transistor may be coupled across transistor 1544. This configuration may provide a higher gate voltage of approximately VDD to signal lines 1516 and 1517 such that node 1533 or 1535 is approximately VDD-VT when a non-masked matching conditions occurs. This may further increase the response time of the CAM cell 1500 by approximately 0.5 to 3 ns.

Figure 18 shows mask-per-bit ternary CAM cell 1800 that is another embodiment of mask-per-bit ternary CAM cell 1320 of Figure 13. CAM cell 1800 includes a CAM cell and a local mask cell. The CAM cell includes memory cell 1806 and compare circuit 1808. The local mask cell includes masking circuit 1810 and mask cell 1812. Memory cell 1806 stores data to be compared with comparand data provided on CL 1310 and CLB 1312 during a compare operation. Memory cell 1806 may be any volatile or nonvolatile memory cell. When memory cell 1806 is selected by word line 1316, data may be read from or written to memory cell 1806 via BL 1306 and BLB 1308.

Masking cell 1812 stores masking data that indicates whether the data stored in memory cell 1806 will be masked during a comparison operation. Masking cell 1812 may be any volatile or nonvolatile memory cell. When masking cell 1812 is selected by mask word line 1318, masking data may be read from or written to masking cell 1812 via BL 1306 and BLB 1308. Masking circuit 1810 receives the masking data from masking cell 1812 over lines 1818 and 1819 and in response thereto determines whether the data stored in memory cell 1806 (provided on lines 1814 and 1815) or masked data is provided to compare circuit 1808 on lines 1816 and 1817.

Compare circuit 1808 compares comparand data on lines CLB 1312 and CL 1310 with data provided by masking circuit 1810 on lines 1816 and 1817. Compare circuit 1808 outputs the comparison result to match line

1314. Compare circuit 1808 may be any type of comparison circuit including an exclusive OR (XOR) or exclusive NOR (XNOR) gate.

When the masking data stored in masking cell 1812 indicates that the data in memory cell 1806 should be masked from a comparison with the comparand data provided on CL 1310 and CLB 1312, masking circuit 1810 provides masked data on lines 1816 and 1817 to compare circuit 1808 such that compare circuit 1808 indicates a match to match line 1314 regardless of whether the data stored in memory cell 1806 matches the comparand data. The masked data provided on lines 1816 and 1817 may be any predetermined data. For one embodiment, the masked data may be the same or the logical complement of the masking data provided on lines 1818 and 1819.

When the masking data stored in masking cell 1812 indicates that the data in memory cell 1806 should not be masked from a comparison with the comparand data, masking circuit 1810 provides the data stored in memory cell 1806 to compare circuit 1808 to compare with the comparand data on CLB 1312 and CL 1310.

Thus, in response to the masking data stored in masking cell 1812, masking circuit 1810 either provides the data stored in memory cell 1806 or masked data to compare circuit 1808. This configuration is also faster in resolving the state of match line 1314 than typical ternary CAM cells such as CAM cell 1600 of Figure 16.

While two signal lines are shown for interfacing between memory cell 1806 and masking circuit 1810 (i.e., lines 1814 and 1815), compare circuit 1808 and masking circuit 1810 (i.e., lines 1816 and 1817), and masking circuit 1810 and masking cell 1812 (i.e., lines 1818 and 1819), any number of signal lines may be used.

Figure 19 shows mask-per-bit ternary CAM cell 1900 that is one embodiment of CAM cell 1800 of Figure 18. CAM cell 1900 includes memory cell 1906, compare circuit 1908, masking circuit 1910, and masking cell 1912 which are exemplary embodiments of circuits 1806, 1808, 1810, and 1812, respectively. Other embodiments may be used.

Memory circuit 1906 includes two cross-coupled inverters 1926 and 1928 that form a bi-stable latch to store data on nodes 1921 and 1923. Data may be communicated between the bi-stable latch and BL 1306 and BLB 1308 via pass gates 1922 and 1924, respectively. Pass gates 1922 and 1924 are controlled by word line 1316. For alternative embodiments, any other type of volatile or nonvolatile memory cell may be used. The data stored by memory cell 1906 is passed on lines 1914 and 1916 to compare circuit 1908 for comparison with the data output by masking circuit 1910.

Masking cell 1912 includes two cross-coupled inverters 1950 and 1952 that form a bi-stable latch to store data on nodes 1945 and 1947. The masking data is communicated between BL 1306 and BLB 1308 via pass gates 1946 and 1948 that are controlled by mask word lines 1318. The masking data stored by the bi-stable latch indicates whether masked data or data stored in memory cell 1906 is provided to compare circuit 1908 for comparison with comparand data.

The masking data is provided to masking circuit 1910 on lines 1918 and 1919. Masking circuit 1910 includes transistors 1938 and 1940 that determine whether masked data or data on line 1914 is provided to line 1916 in response to the masking data on lines 1918 and 1919. Transistor 1938 has its source coupled to ground, its drain coupled to line 1916, and its gate coupled to line 1918. Transistor 1940 has its drain (source) coupled to line 1916, its source (drain) coupled to line 1914, and its gate coupled to line 1919. Masking circuit 1910 further includes transistors 1942 and 1944 that determine whether masked data or data on line 1915 is provided to line 1917 in response to the masking data on lines 1918 and 1919. Transistor 1944 has its source coupled to ground, its drain coupled to line 1917, and its gate coupled to line 1918. Transistor 1942 has its drain (source) coupled to line 1917, its source (drain) coupled to line 1915, and its gate coupled to line 1919.

Compare circuit 1908 includes two sets of transistors to compare the data output by memory cell 1906 on signal lines 1914 and 1915 with the comparand data on CLB 312 and CL 310. The first set of transistors includes transistors 1930 and 1932. Transistor 1930 has its source coupled to ground,

its drain coupled to the drain (source) of transistor 1932, and its gate coupled to signal line 1916. Transistor 1932 has its source (drain) coupled to match line 1314 and its gate coupled to CLB 1312. The second set of transistors includes transistors 1934 and 1936. Transistor 1934 has its source coupled to ground, its drain coupled to the drain (source) of transistor 1936, and its gate coupled to signal line 1917. Transistor 1936 has its gate coupled to CL 1310 and its source (drain) coupled to match line 1314. Match line 1314 may be precharged to a voltage approximately equal to a power supply voltage VDD by precharge circuit 1920.

The operation of CAM cell 1900 may be illustrated as follows. When masking is disabled, masking cell 1912 provides a logic zero signal on line 1918 to turn off transistors 1938 and 1944, and further provides a logic one signal on line 1919 to enable transistors 1940 and 1942 to provide the data on lines 1914 and 1915 to lines 1916 and 1917, respectively. Thus, when masking is disabled, compare circuit 1908 compares the data on lines 1914 and 1915 with the comparand data from CLB 1312 and CL 1310, respectively. If there is a match, neither set of transistors in compare circuit 1908 will provide a path to ground and the state of match line 1314 will remain unaltered. If there is no match, then match line 1314 will be discharged towards ground through at least one of the sets of transistors in compare circuit 1908.

When masking is enabled, masking cell 1912 provides a logic zero signal on line 1919 to turn off transistors 1940 and 1942 such that the memory cell data is not provided to signal lines 1916 and 1917. Additionally, masking cell 1912 provides a logic one signal on signal line 1918 to turn on transistors 1938 and 1944 and pull lines 1916 and 1917 towards a ground potential. When signal lines 1916 and 1917 are pulled towards a ground potential, transistors 1930 and 1934 are turned off such that no path to ground is available in compare circuit 1908 regardless of whether the comparand data on CLB 1312 and CL 1310 matches the data stored by memory cell 1906. Thus, the comparison operation is masked.

As with ternary CAM cell 1500, masking circuit 1910 is not used to gate a completed comparison to match line 1314; rather, CAM cell 1900 uses masking circuit 1910 to determine the data supplied to compare circuit 1908. Thus, match line 1314 may be charged and discharged faster than other ternary CAM cell architectures. For example, consider the case where match line 1314 is initially precharged to a high logic state and one or more ternary CAM cells such as CAM cell 1900 indicate a non-masked matching condition. During a comparison operation, the non-masked matching cells will each have an intermediate node 1933 or 1935 that will charge to approximately VDD-VT, while node 1937 remains precharged to approximately VDD by precharge circuit 1920. If one of the ternary CAM cells coupled to the same match line subsequently indicates a non-masked mismatching condition in a subsequent compare operation, then the non-masked mismatching cell will need to discharge match line 1314 and the intermediate nodes 1933 (and/or 1935) of the non-masked matching cells. Note that only one intermediate node 1933 or 1935 will have to be discharged rather than two intermediate nodes as illustrated in ternary CAM cell 1600 of Figure 16. Similarly, if the non-masked mismatching cell subsequently indicates a non-masked matching condition in a subsequent compare operation, then only one intermediate node 1933 or 1935 will need to be charged to VDD-VT by the precharge circuit 1920 and the other non-masked matching cells. This can result in a significant decrease in the time required to resolve the state of match line 1314 and thus may result in a significant decrease in the time required to generate a match flag for the CAM device.

The response time of CAM cell 1900 may be further increased by placing PMOS transistors across transistors 1940 and 1942. For example, a PMOS transistor may have source (drain) coupled to the source (drain) of transistor 1940 and line 1914, its drain (source) coupled to the drain (source) of transistor 1940 and signal line 1916, and its gate coupled to signal line 1918. A similarly configured PMOS transistor may be coupled across transistor 1942. This configuration may provide a higher gate voltage of

approximately VDD to signal lines 1916 and 1917 such that node 1933 or 1935 is approximately VDD-VT when a non-masked matching conditions occurs. This may further increase the response time of the CAM cell 1500.

Figure 20 shows ternary CAM cell 2000 that is another embodiment of CAM cell 1800 of Figure 18. CAM cell 2000 includes a compare circuit 1908 that is the same as for CAM cell 1900 of Figure 19, but includes a different masking circuit 2010. Masking circuit 2010 includes two NOR gates 2002 and 2004 that provide either masked data or the data stored in memory cell 1806 to lines 1816 and 1817 in response to masking data stored in masking cell 1812 and provided on line 1819. NOR gate 2002 has a first input coupled to signal line 1814, a second input coupled to the masking data on line 1819, and an output coupled to the gate of transistor 1930 via signal line 1816. NOR gate 2004 has a first input coupled to signal line 1815, a second input coupled to the masking data on line 1819, and an output coupled to the gate of transistor 1934 via signal line 1817. When the masking data is a logic zero on signal line 1819, masking is disabled and the logical complement of the data stored in memory cell 1806 is provided to compare circuit 1908 for comparison with the comparand data on CLB 1312 and CL 1310. When the masking data is a logic one on signal line 1819, masking is enable and masked data is provided to compare circuit 1908 such that match line 1314 cannot be discharged. For other embodiments, one or more other logic gates may be used in place of NOR gates 2002 and 2004, and one or more signals may be generated by masking cell 1812.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

CLAIMS

What is claimed is:

1. A content addressable memory (CAM) cell for coupling to a match line, the CAM cell comprising:
 - a first memory cell for storing first data;
 - a second memory cell for storing masking data;
 - a masking circuit to receive comparand data and said masking data, and to output second data ; and
 - a compare circuit coupled to said memory cell and said masking circuit, said compare circuit to compare said first data and said second data to affect a logical state of said match line.
2. The CAM circuit of claim 1, wherein said second data comprises said comparand data.
3. The CAM circuit of claim 1, wherein said second data comprises masked data generated in response to said masking data.
4. The CAM circuit of claim 1, further comprising:
 - a word line coupled to said first memory cell;
 - a first bit line coupled to said first memory cell;
 - a second bit line coupled to said first memory cell;
 - a first comparand line coupled to said masking circuit; and
 - a second comparand line coupled to said masking circuit.
5. The CAM circuit of claim 4, further comprising:
 - a mask word line coupled to said second memory cell;
 - a first mask bit line coupled to said second memory cell; and
 - second mask bit line coupled to said second memory cell.
6. The CAM circuit of claim 1, wherein said masking circuit comprises:
 - a first transistor having a source coupled to ground, a drain coupled to an input of said compare circuit, and a gate coupled to said masking data; and
 - a second transistor having a source coupled to the drain of said first transistor, a drain coupled to said input of said compare circuit, and a gate coupled to said masking data.

7. A content addressable memory (CAM) circuit for coupling to a match line, the CAM circuit comprising:
 - a first memory cell for storing memory data;
 - a second memory cell for storing masking data
 - a masking circuit having inputs to receive said memory data and said masking data, and further having an output to provide first data; and
 - a compare circuit coupled to said masking circuit, said compare circuit to compare said first data and comparand data to affect a logical state of said match line.
8. The CAM circuit of claim 7, wherein said first data comprises said memory data.
9. The CAM circuit of claim 7, wherein said first data comprises mask data generated in response to said masking data.
10. The CAM circuit of claim 7, further comprising:
 - a word line coupled to said first memory cell;
 - a first bit line coupled to said first memory cell;
 - a second bit line coupled to said first memory cell;
 - a first comparand line coupled to said masking circuit; and
 - a second comparand line coupled to said masking circuit.
11. The CAM circuit of claim 10, further comprising:
 - a mask word line coupled to said second memory cell;
 - a first mask bit line coupled to said second memory cell; and
 - a second mask bit line coupled to said second memory cell.
12. The CAM circuit of claim 7, wherein said masking circuit comprises
 - a first transistor having a source coupled to ground, a drain coupled to an input of said compare circuit, and a gate coupled said second memory cell; and
 - a second transistor having a source coupled to said first memory cell, a drain coupled to the drain of said first transistor, and a gate coupled to said second memory cell.
13. The CAM circuit of claim 7, wherein said masking circuit comprises a NOR gate.

14. A method of operating a content addressable memory (CAM) device, said method comprising:
 - providing first data from a memory cell to a compare circuit;
 - providing second data from a masking circuit to said compare circuit;
 - comparing said first data and said second data; and
 - determining a logical state of a match line in response to said comparison.
15. The method of claim 14 wherein said second data comprises comparand data.
16. The method of claim 14 wherein said second data comprises masked data.
17. A method of operating a content addressable (CAM) device, said method comprising:
 - providing first data from a masking circuit to a compare circuit;
 - providing comparand data to said compare circuit;
 - comparing said first data with said second data; and
 - determining a logical state of a match line in response to said comparison.
18. The method of claim 17 wherein said first data comprises data stored in a memory cell.
19. The method of claim 17 wherein said first data comprises masked data.
20. A method of accessing data from a synchronous content addressable memory (CAM) device, comprising:
 - loading data into a plurality of CAM cells in the CAM device;
 - loading individual mask data for each of the plurality of CAM cells in the CAM device;
 - instructing the CAM device to compare comparand data with data stored in a plurality of first CAM cells;

comparing the comparand data with the data stored in each of the plurality of CAM cells that is not masked by the individual mask data;
sensing the data stored in CAM cell; and
outputting the sensed data from the CAM device, wherein the instructing, comparing, sensing, and outputting steps all occur in less than three clock cycles.

21. A method of accessing data from a synchronous content addressable memory (CAM) device, comprising:

instructing the CAM device to compare comparand data with data stored in a plurality of first individually maskable CAM cells;
comparing the comparand data with the data stored in the plurality of first individually maskable CAM cells;
determining a match address for at least one of the plurality of CAM cells storing data matching the comparand data; and
outputting the match address from the CAM device, wherein the instructing, comparing, determining, and outputting steps all occur in less than three clock cycles.

22. A synchronous content addressable memory (CAM) device comprising:

a CAM array having a plurality of individually maskable CAM cells each including a memory cell to store data and a mask cell to store masking data, the CAM array also including a plurality of match lines;
a clock input for receiving a clock signal;
an encoder coupled to the CAM array for encoding signals on the match lines and generate an encoded match address;
an address decoder coupled to receive the encoded match address and provide a decoded match address to the CAM array; and
an instruction decoder coupled to the CAM array and the clock input, the instruction decoder to receive an instruction that instructs the CAM device to compare comparand data with the data stored in the memory cells of the individually masked CAM cells and output a CAM address of a

matching location in less than three clock cycles after receiving the instruction.

23. The synchronous CAM device of claim 22, further comprising a timing generator coupled to the instruction decoder and the clock input, the timing generator for outputting a plurality of signals to the comparand storage element, the encoder and the address decoder.

24. The synchronous CAM device of claim 22, wherein the encoder comprises a priority encoder.

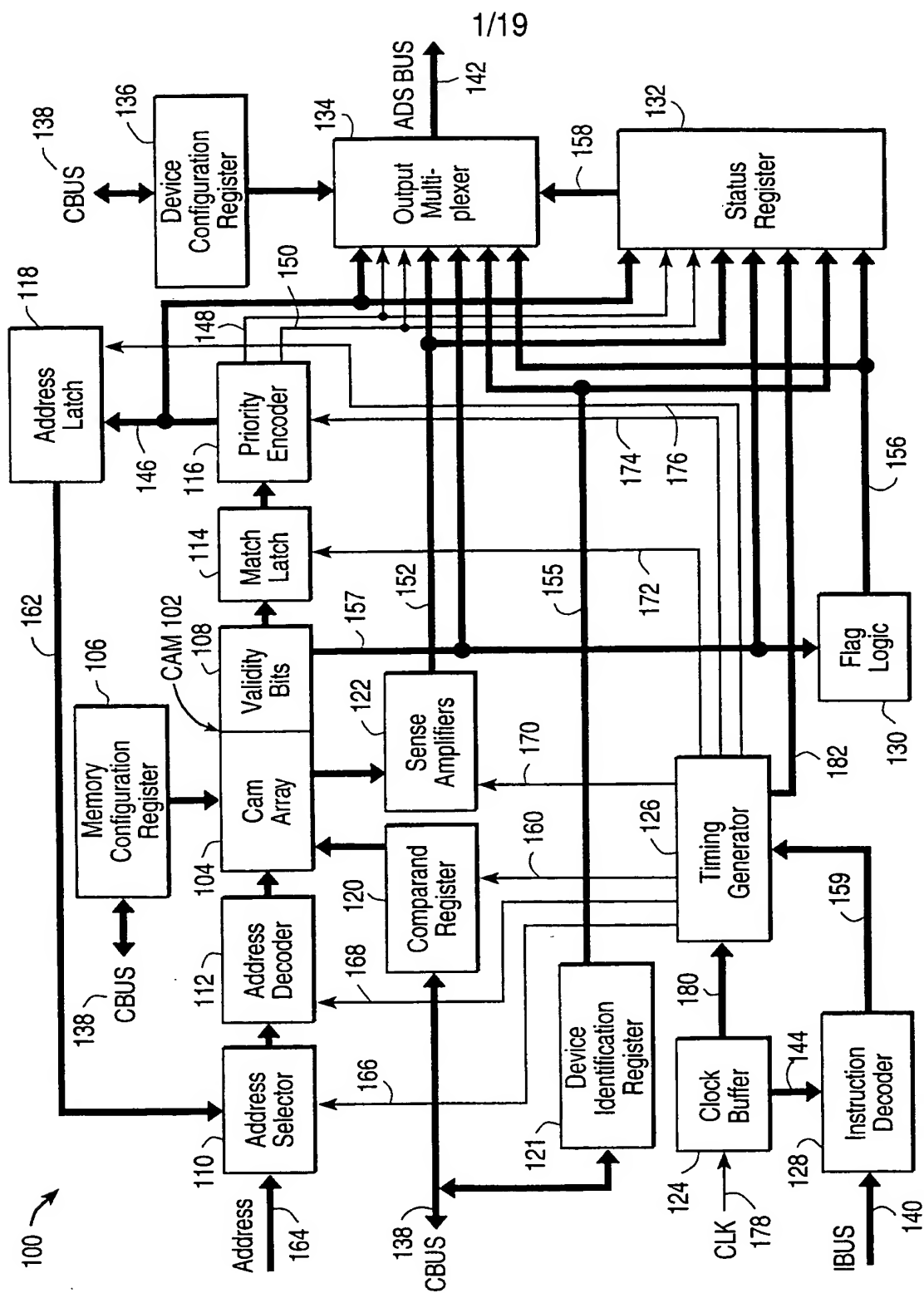


FIG. 1

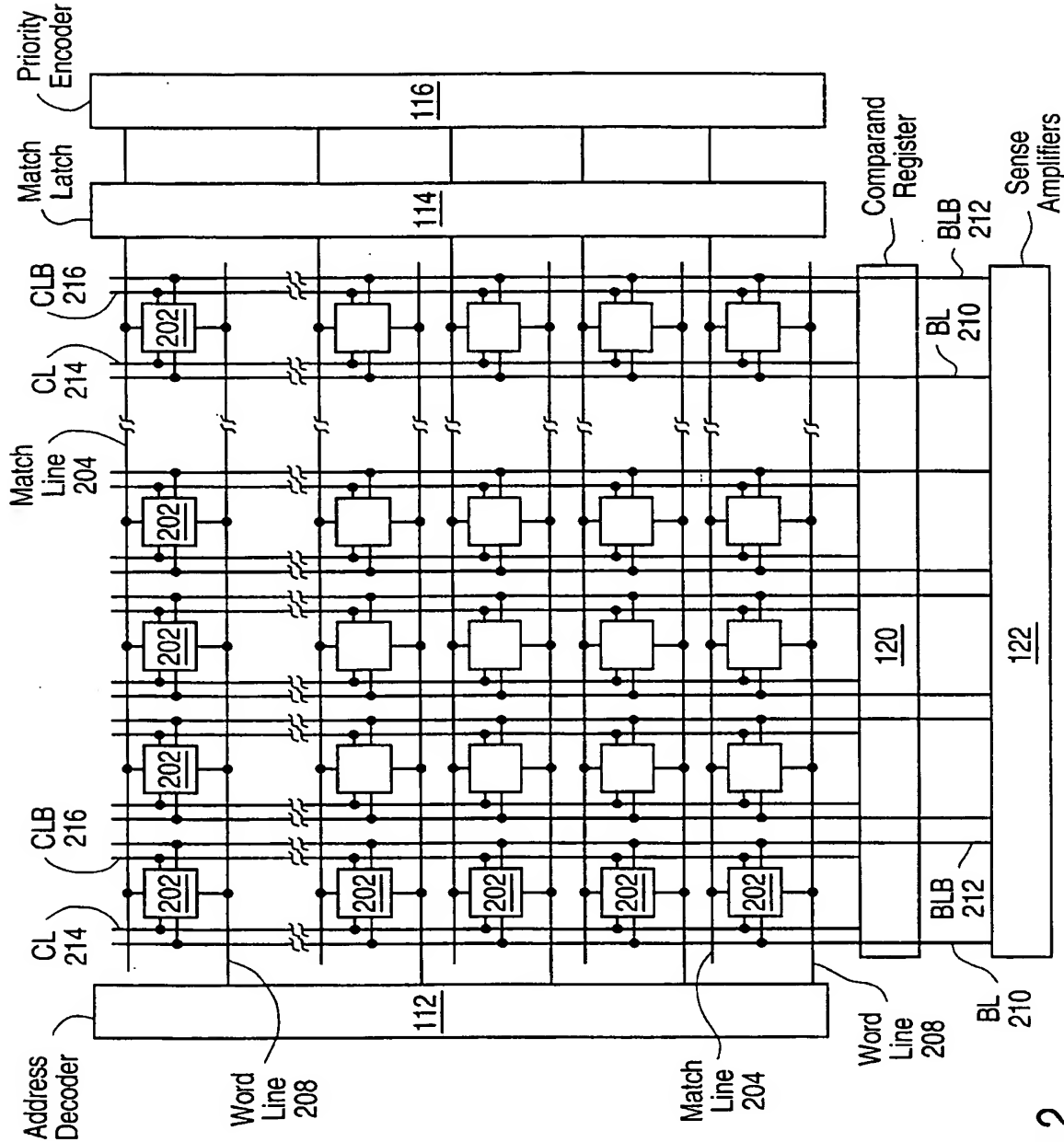


FIG. 2

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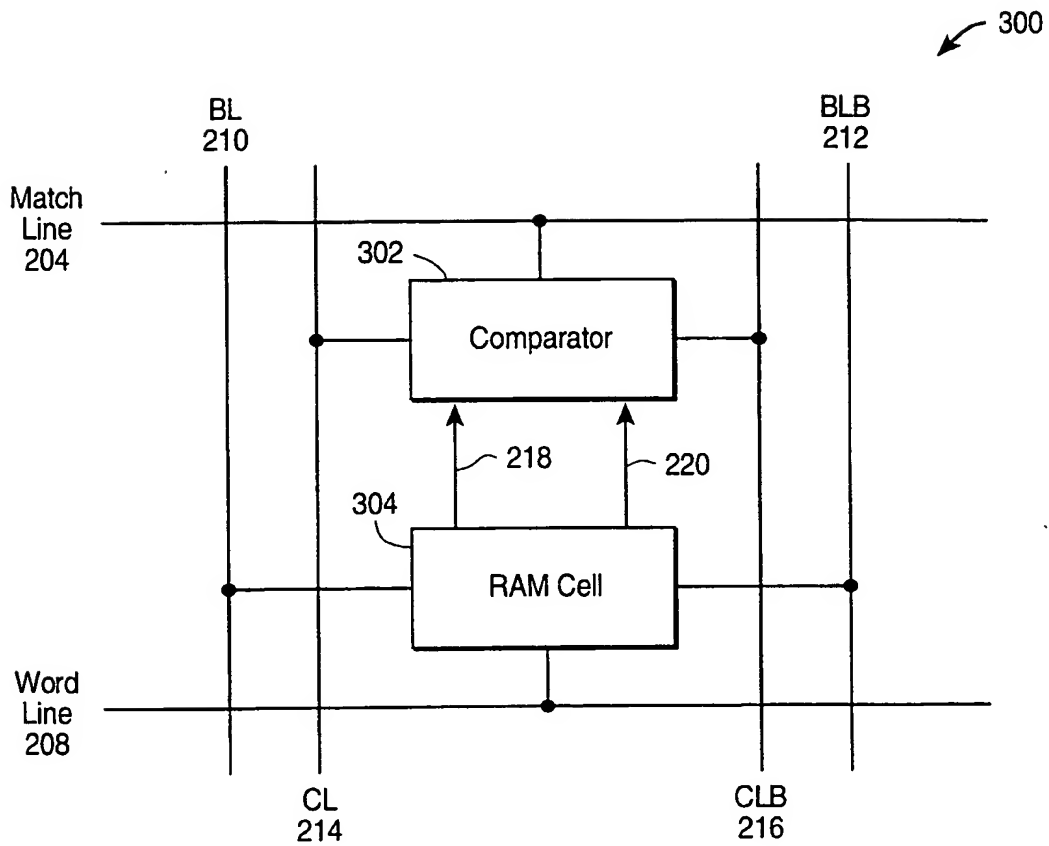


FIG. 3

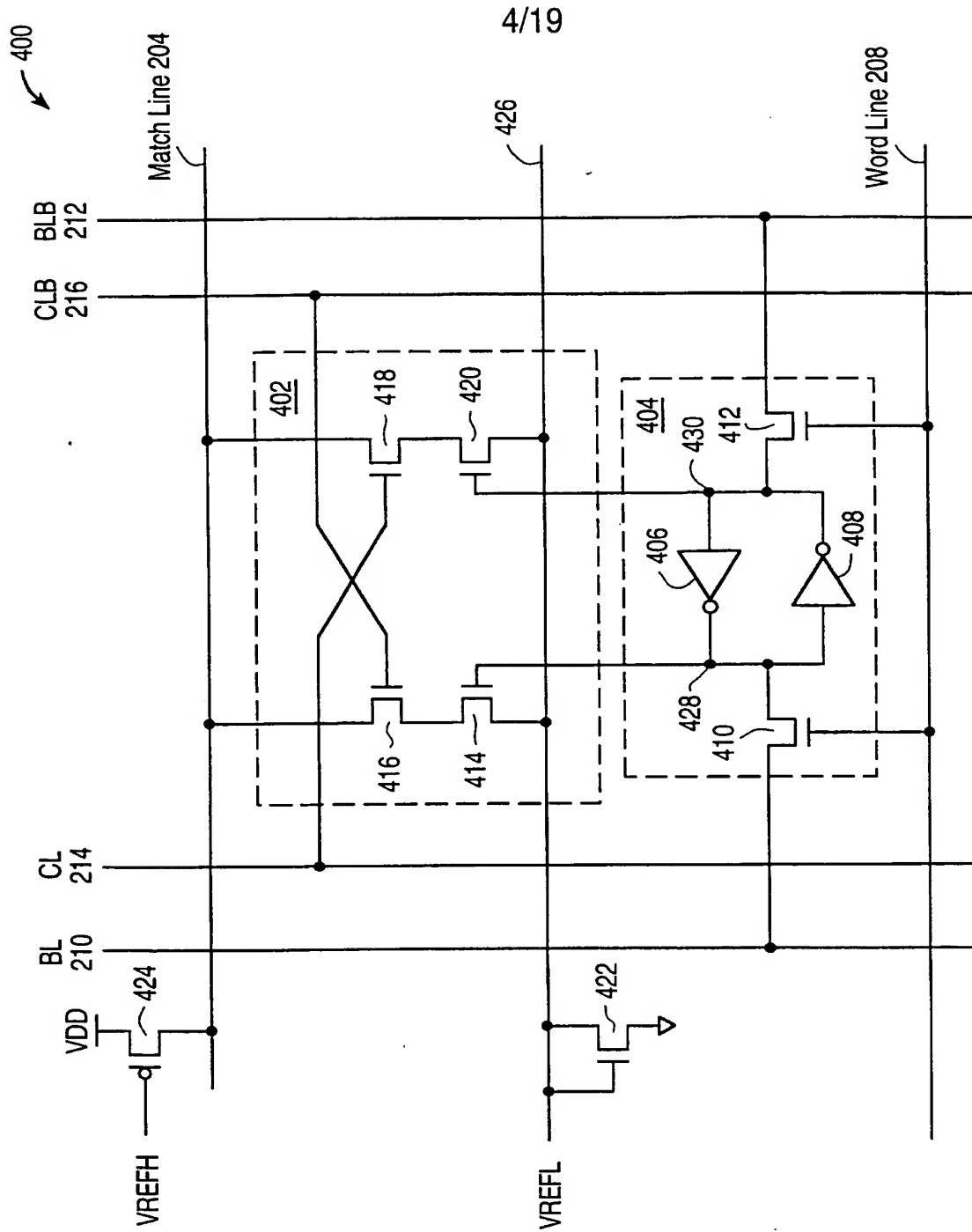


FIG. 4

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500

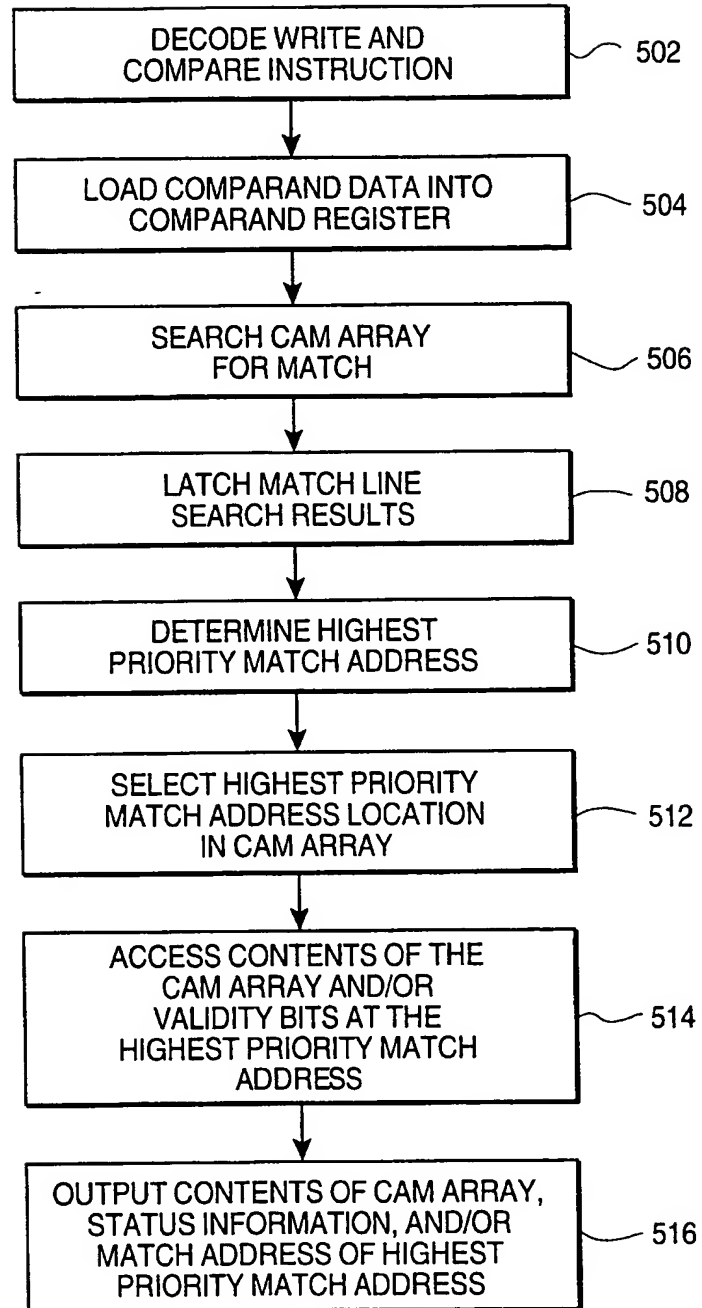


FIG. 5

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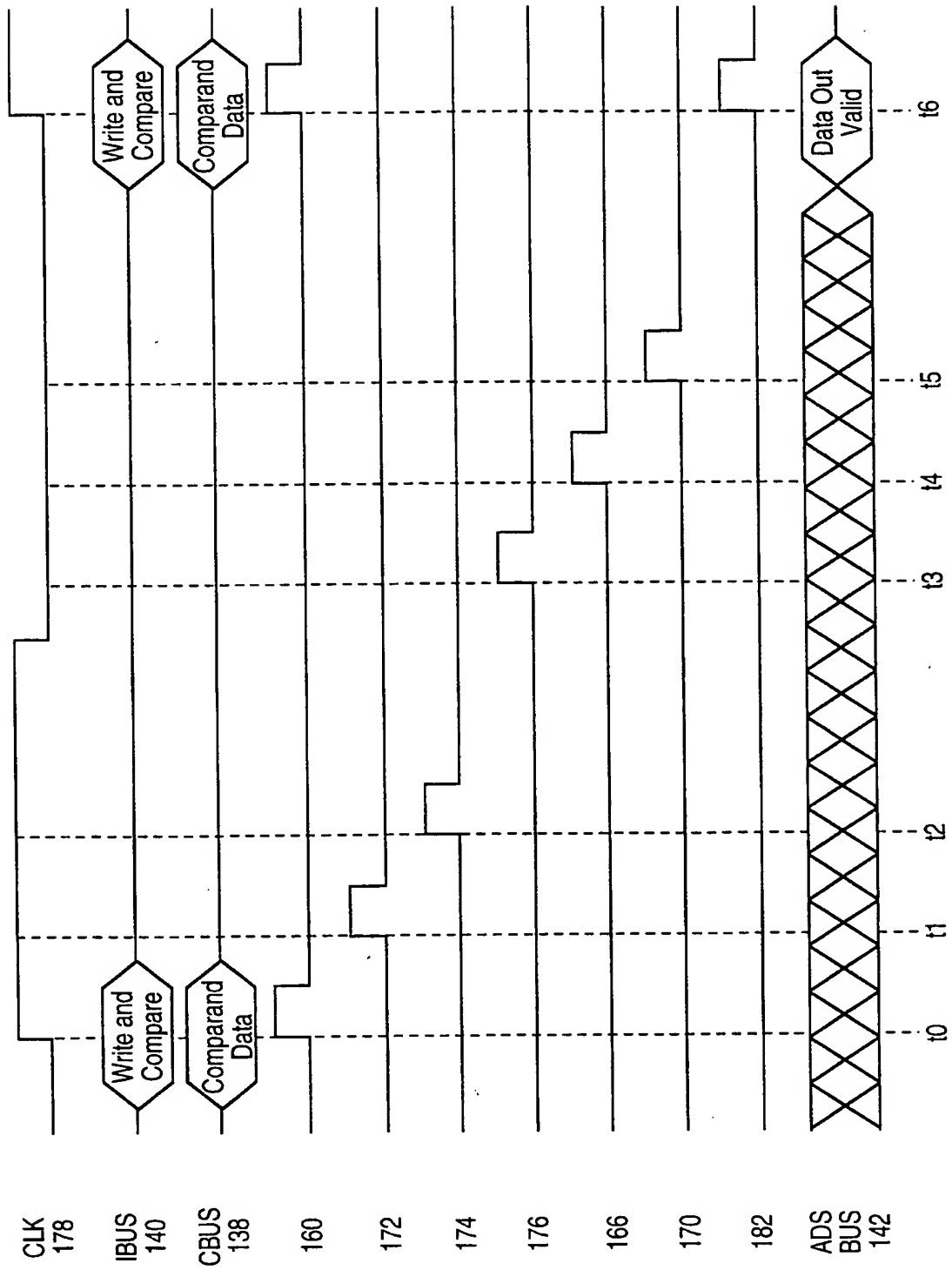


FIG. 6

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700

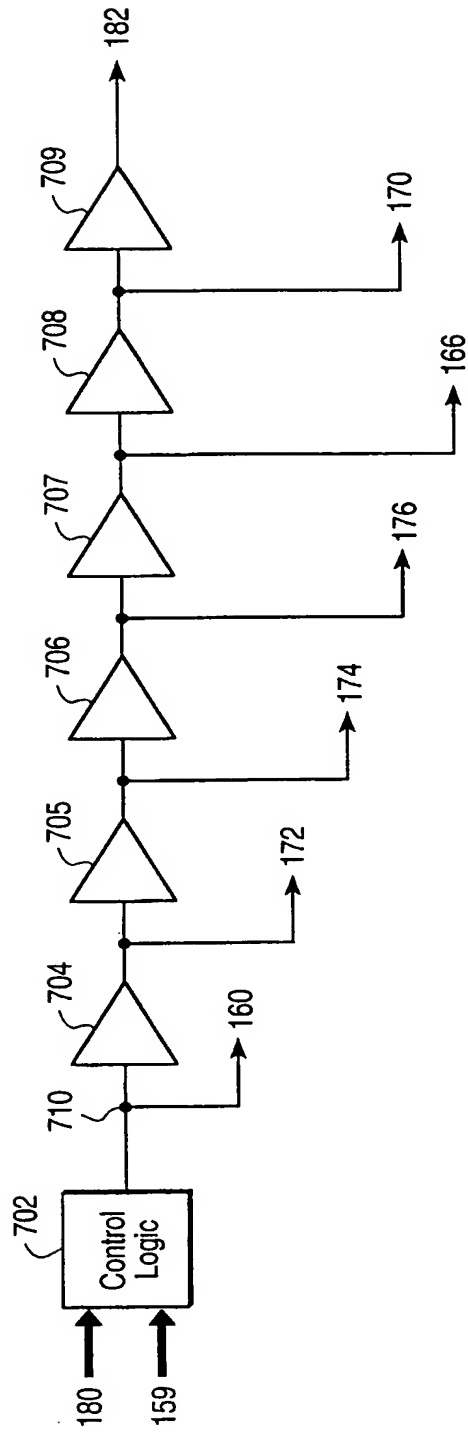


FIG. 7

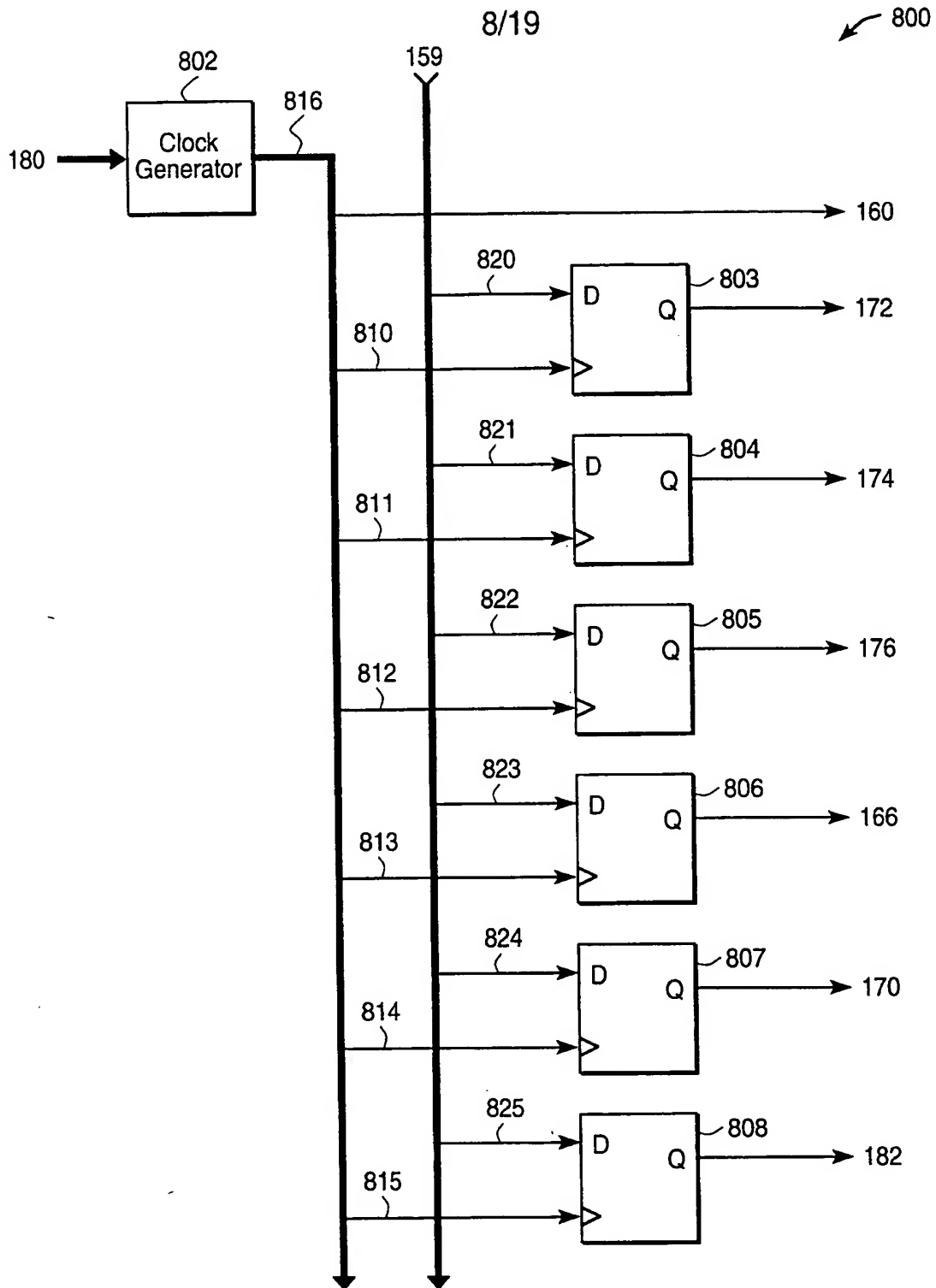


FIG. 8

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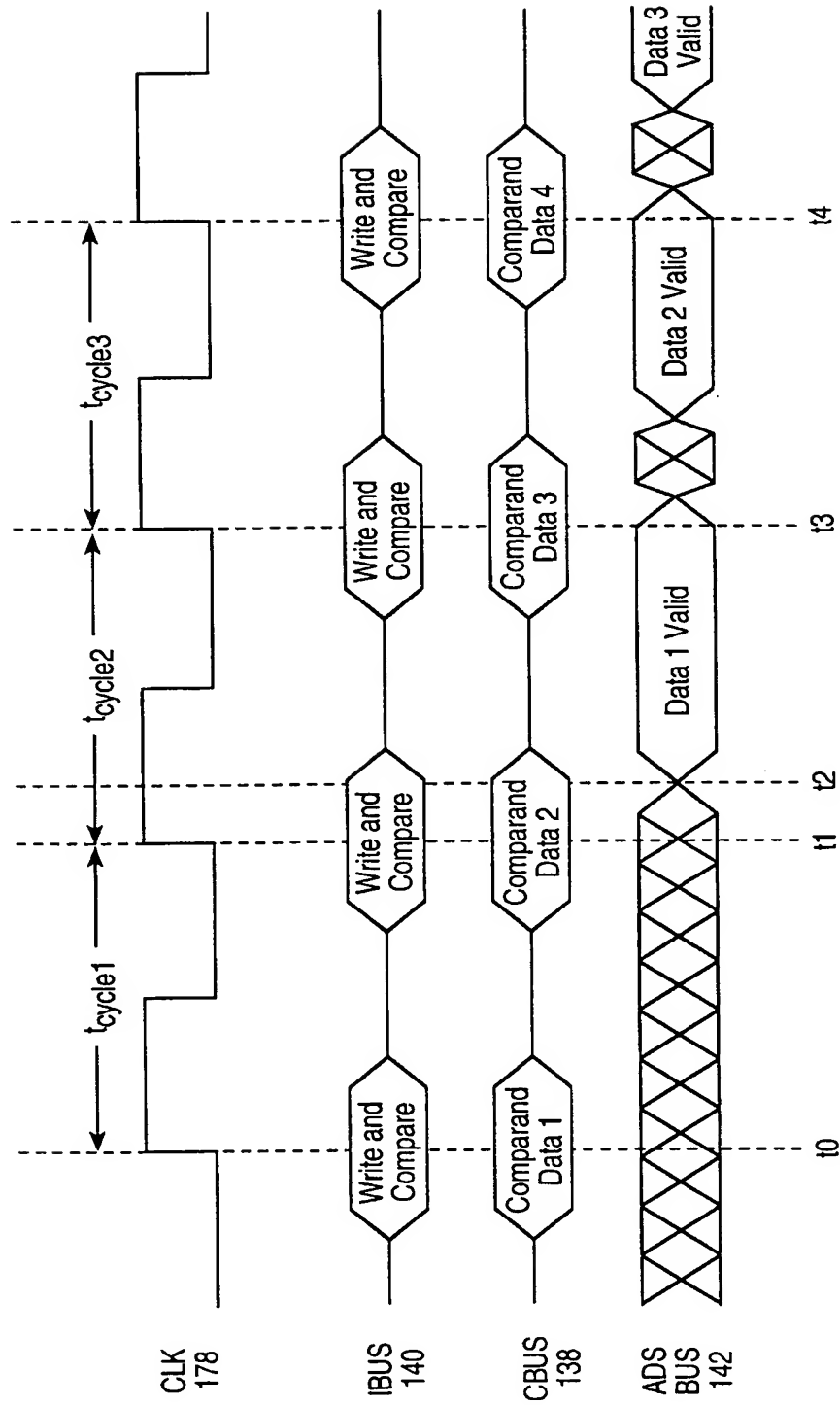


FIG. 9

Bit 63	...	Bit 52	Bit 51	...	Bit 40	Bit 39	...	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32	Bit 31	...	Bit 0
Match Address			Device ID			Reserved			MF	MMF	FF	Skip	Empty	Data from Cam Array 104		

FIG. 10

Bit 63	...	Bit 52	Bit 51	...	Bit 48	Bit 47	...	Bit 0
Match Address			Device ID			Data from Cam Array 104		

FIG. 11

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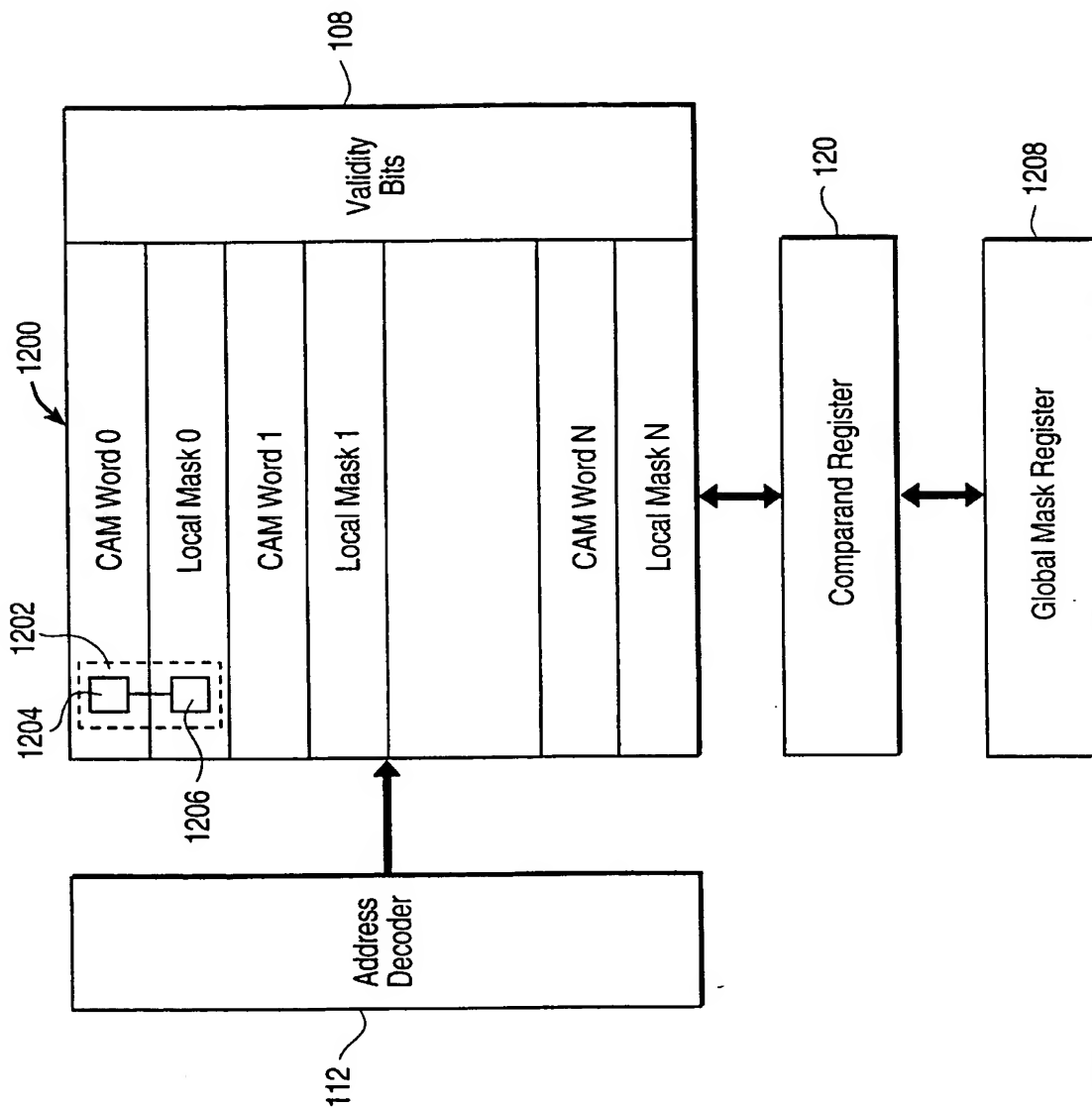


FIG. 12

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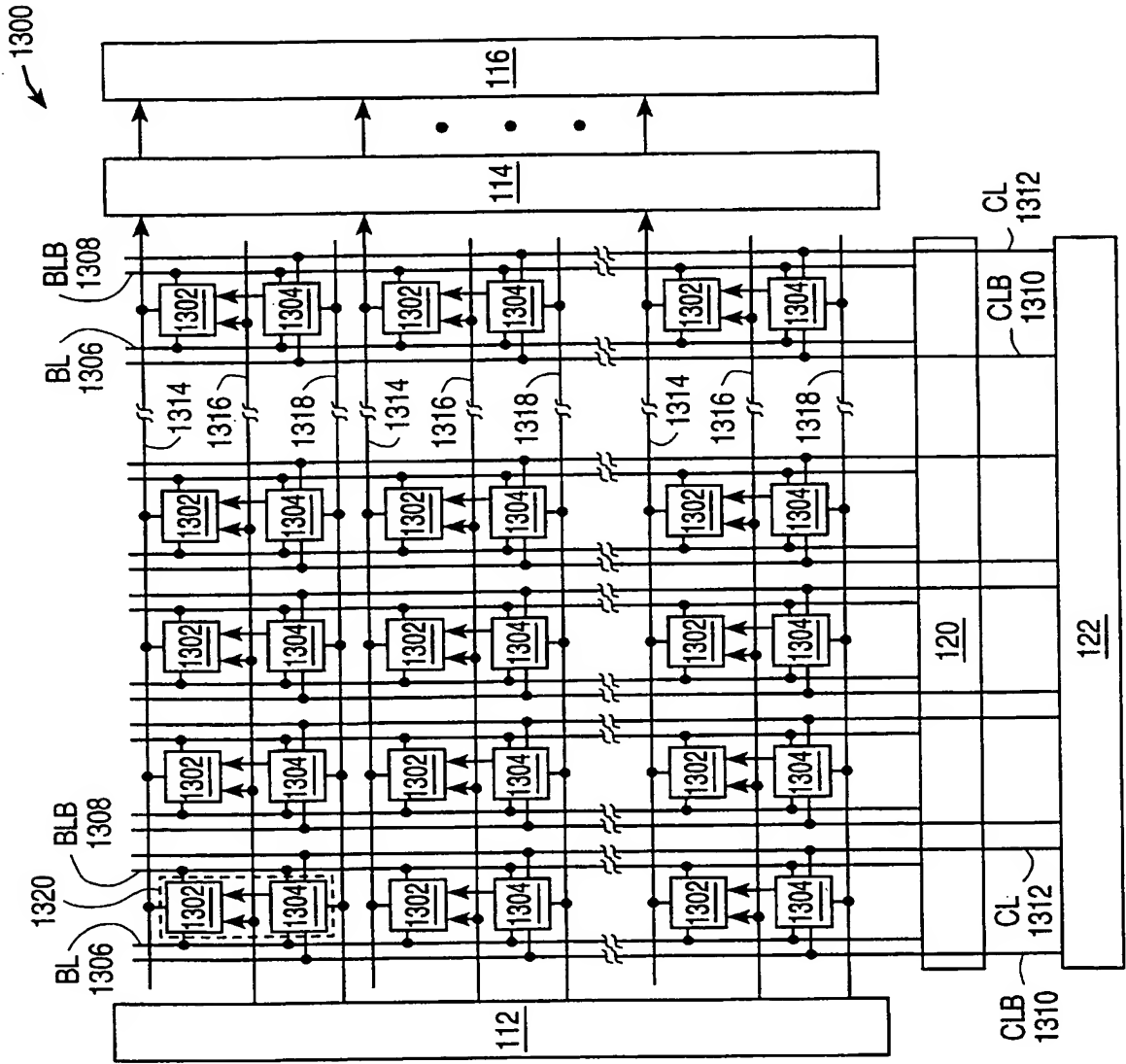


FIG. 13

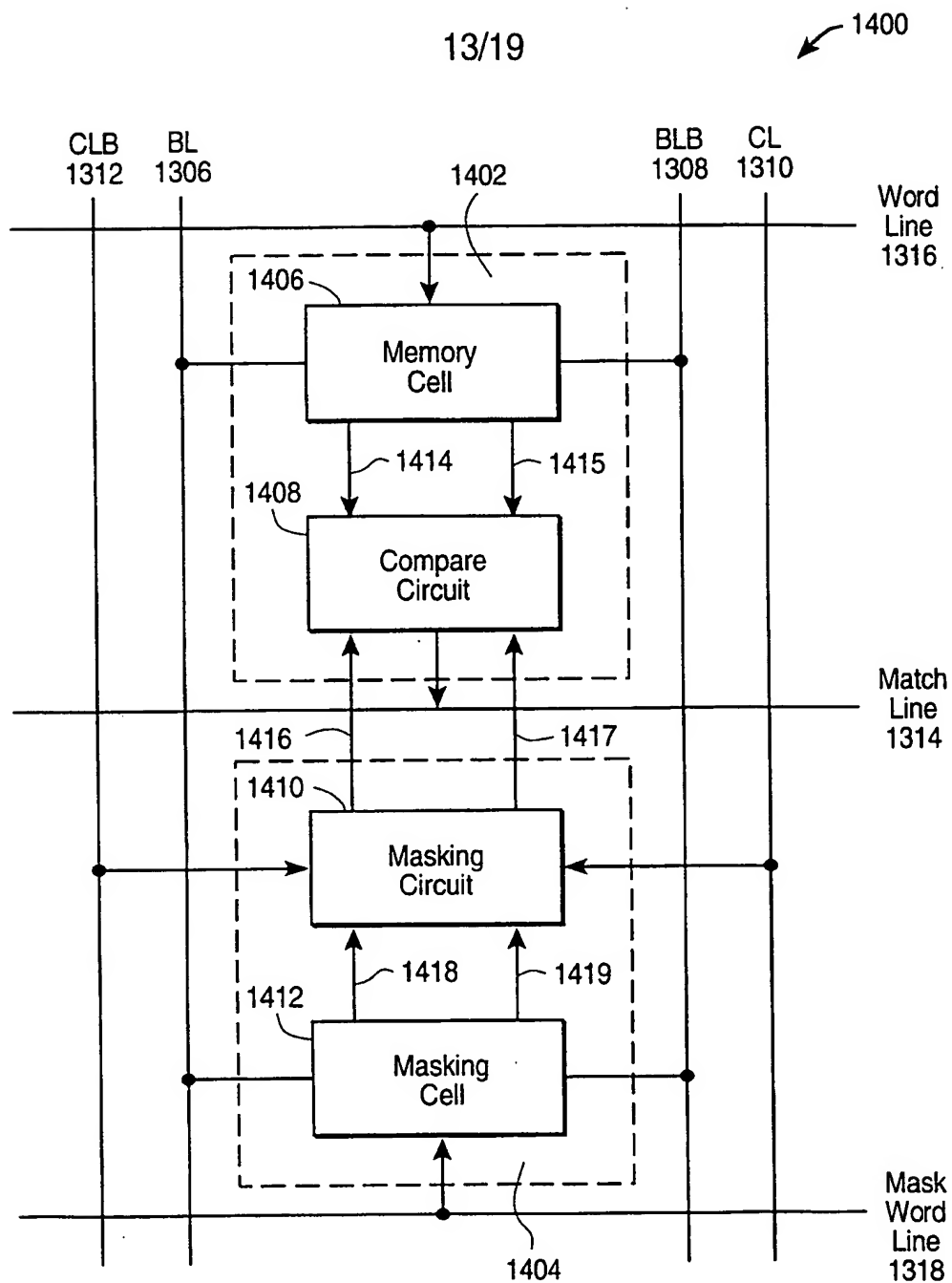


FIG. 14

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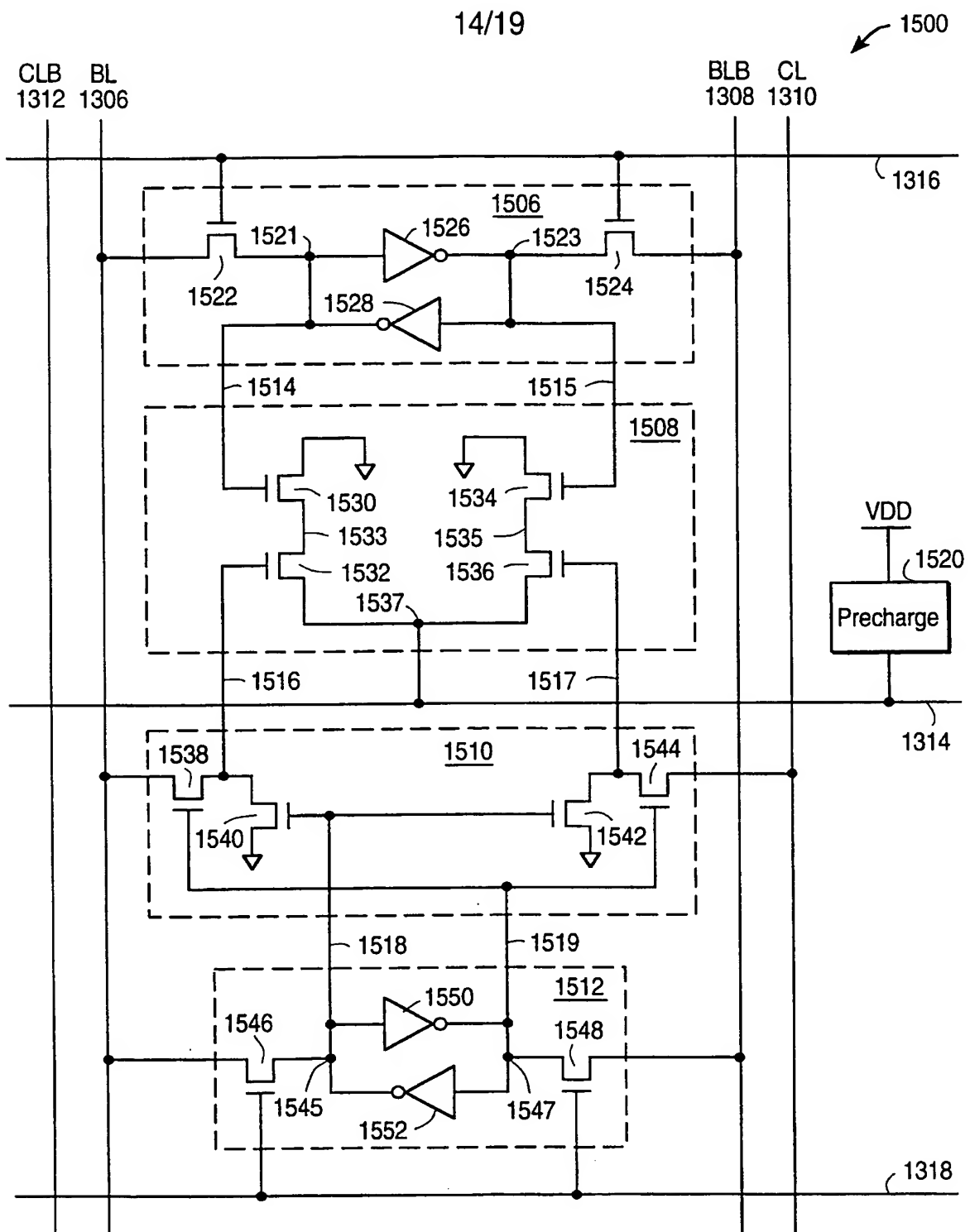


FIG. 15

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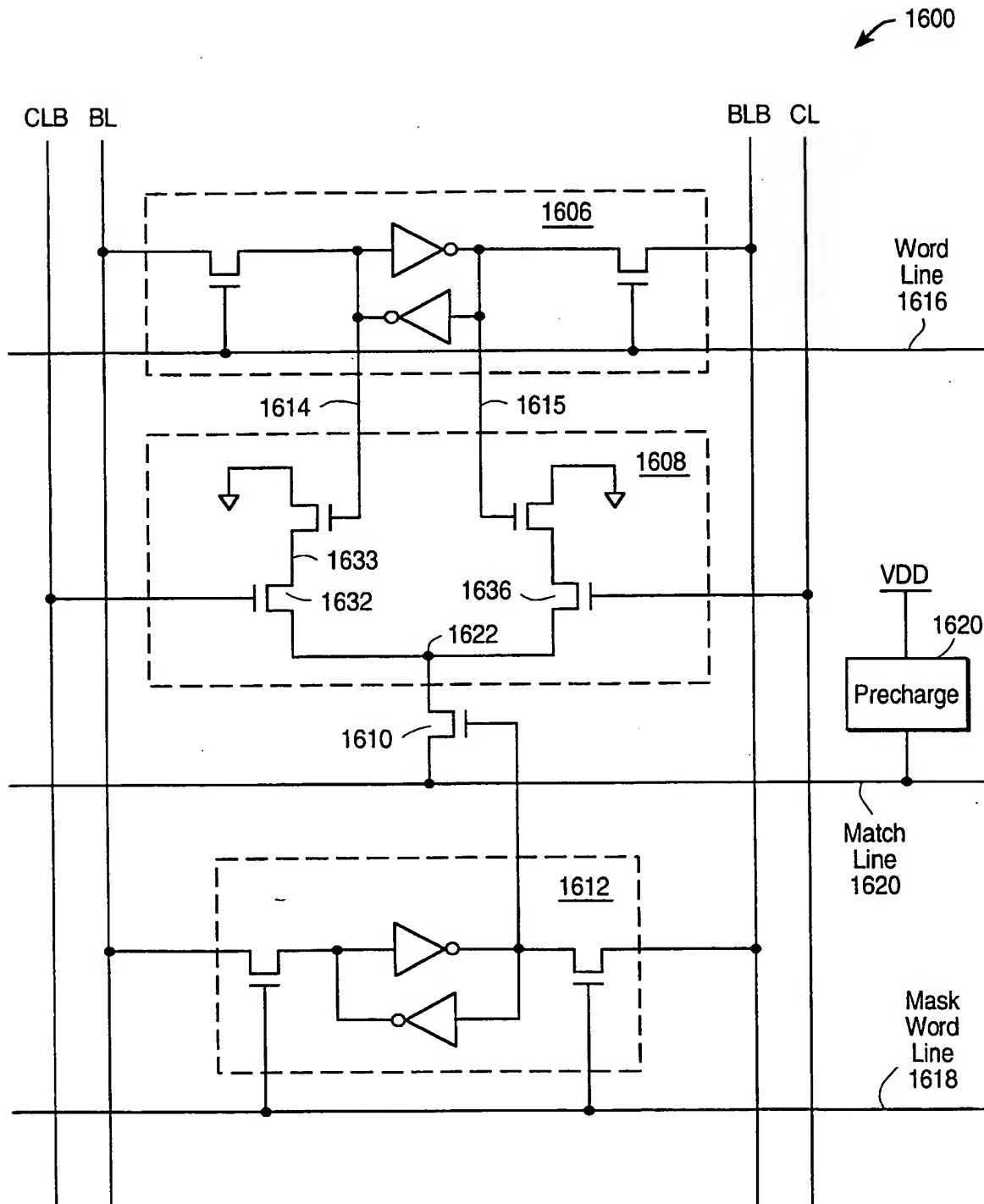


FIG. 16

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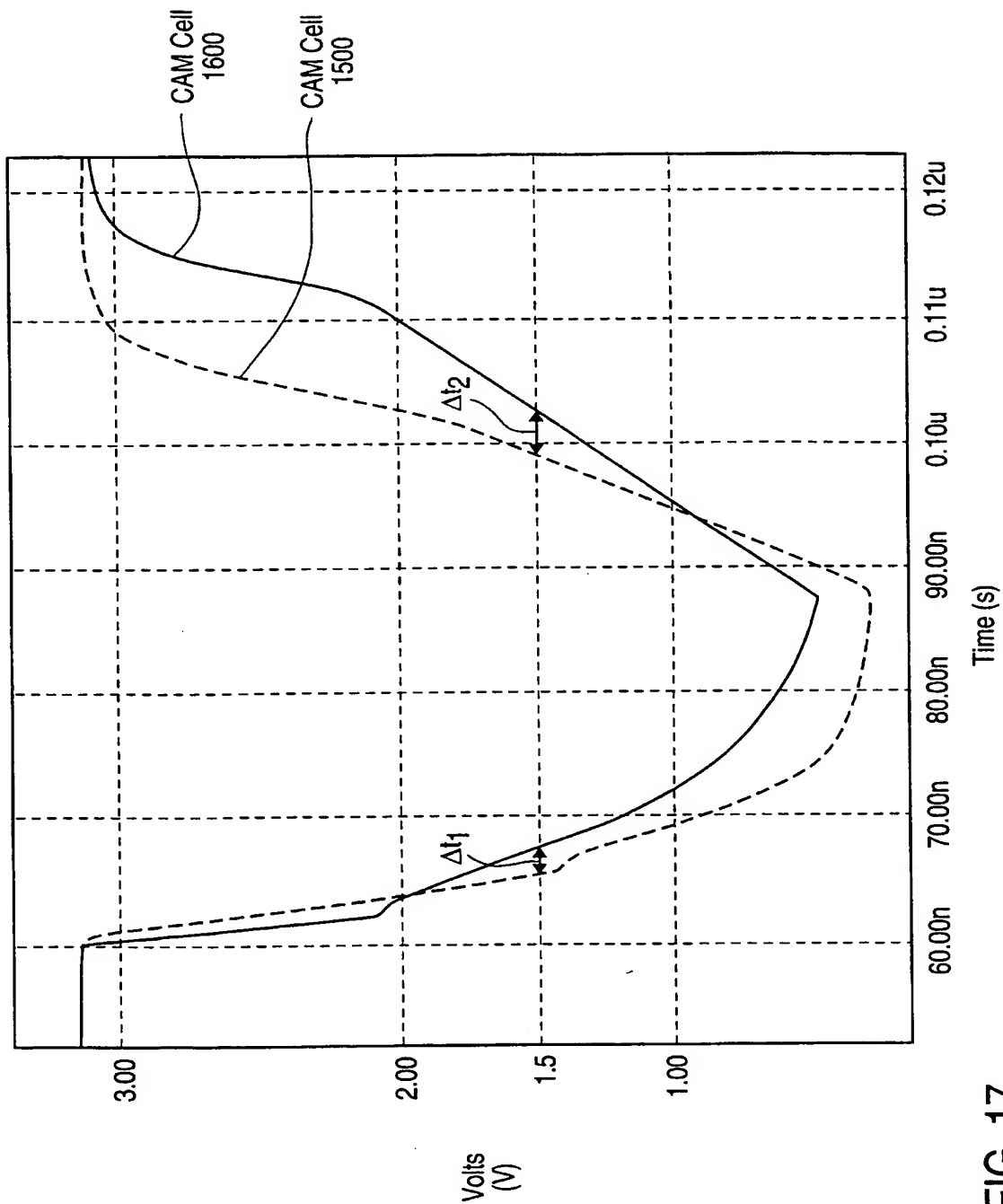


FIG. 17

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1800

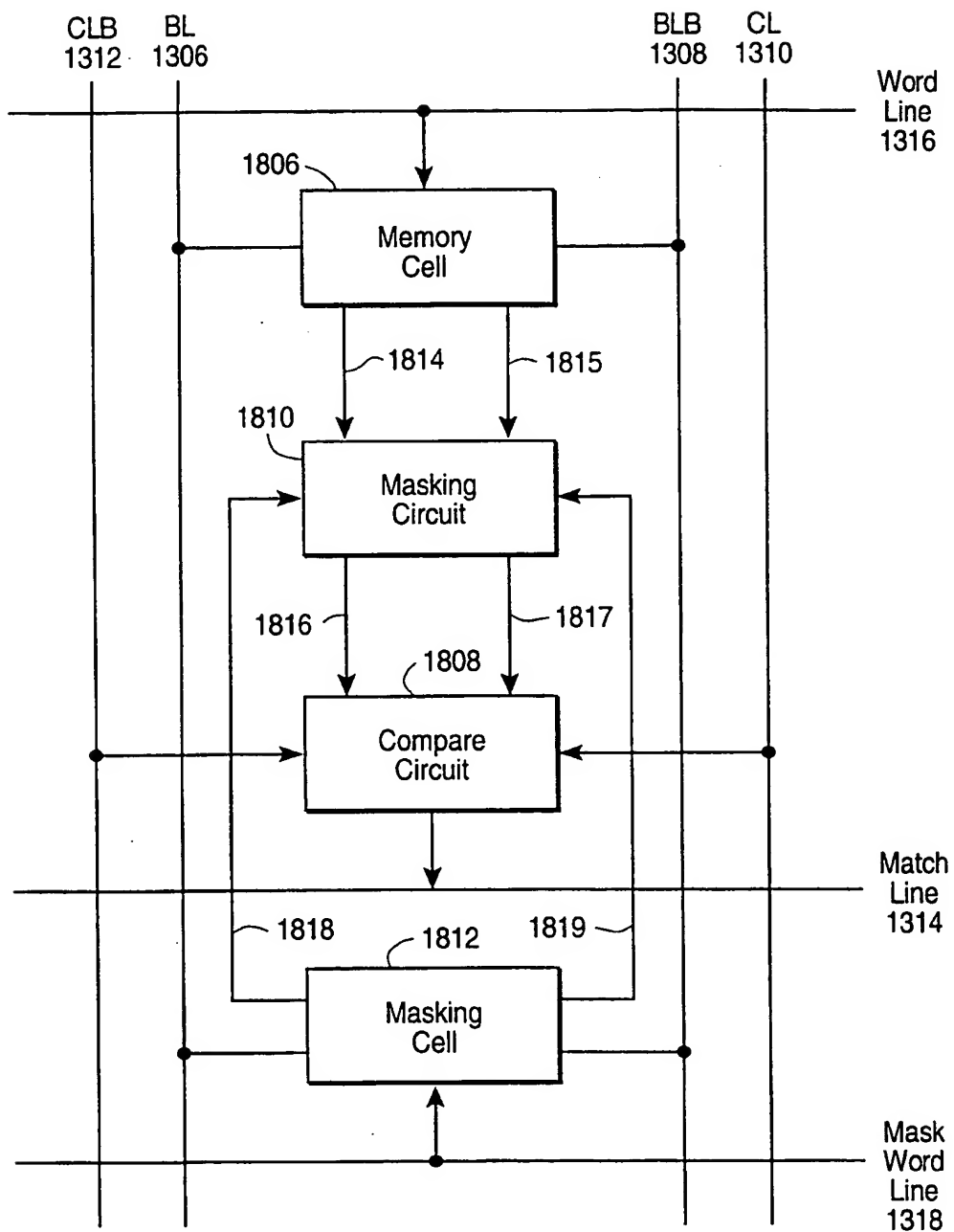


FIG. 18

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1900

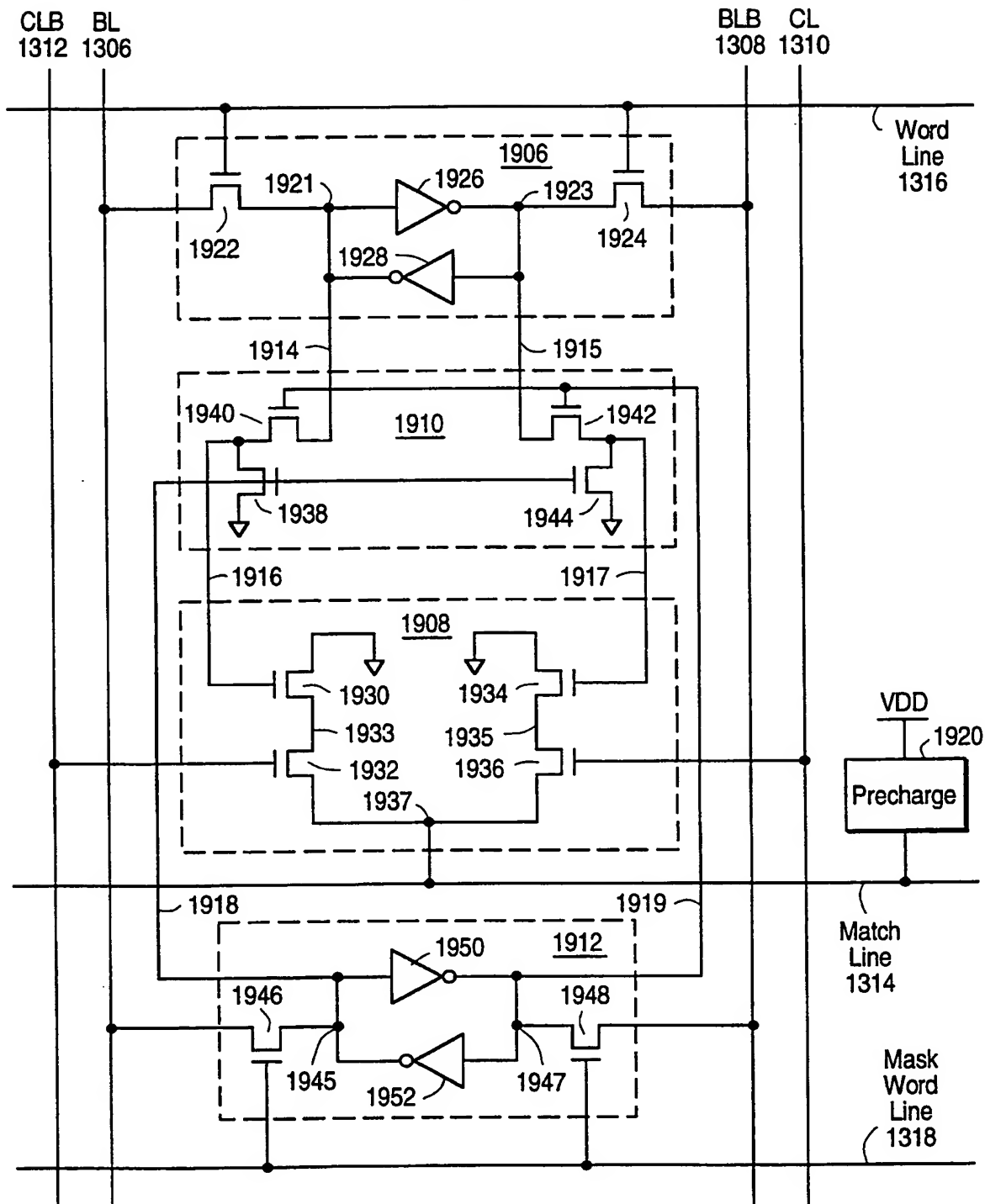


FIG. 19

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19/19

2000

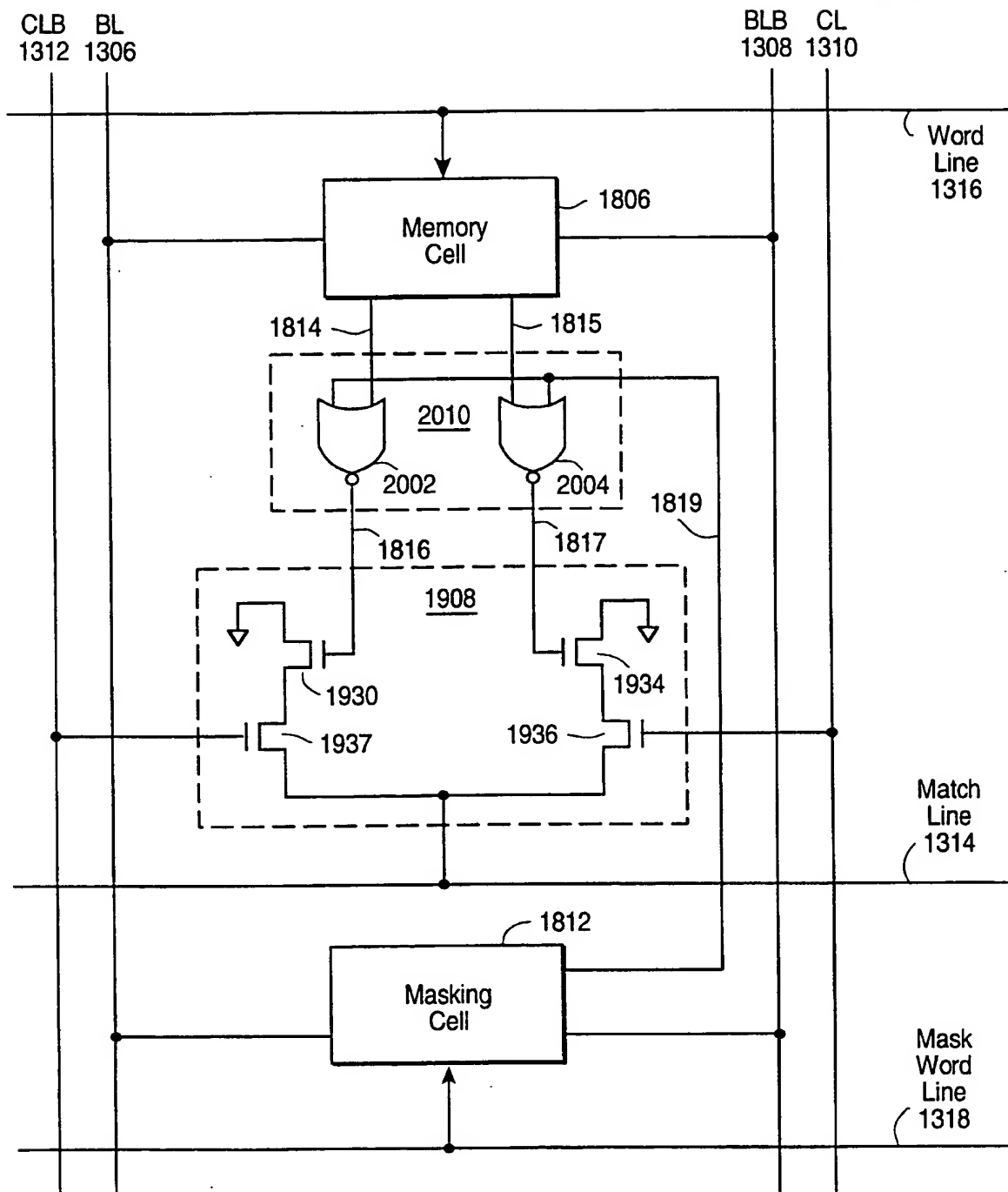


FIG. 20

INTERNATIONAL SEARCH REPORT

1. International Application No.

PCT/US 98/21853

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G11C15/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 226 005 A (LEE DAVID C ET AL) 6 July 1993 see the whole document ---	1-24
A	EP 0 660 332 A (HAL COMPUTER SYSTEMS INC) 28 June 1995 see abstract; figure 3 -----	1

☐ Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"S" document member of the same patent family

Date of the actual completion of the international search

29 January 1999

Date of mailing of the international search report

04/02/1999

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INTERNATIONAL SEARCH REPORT

Information on patent family members

national Application No

PCT/US 98/21853

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5226005 A	06-07-1993	DE 69125393 D	30-04-1997
		DE 69125393 T	04-09-1997
		EP 0558654 A	08-09-1993
		JP 6502737 T	24-03-1994
		WO 9209086 A	29-05-1992
EP 0660332 A	28-06-1995	US 5319590 A	07-06-1994